17.5 All-Digital PLL and GSM/EDGE Transmitter in 90nm CMOS

Robert Bogdan Staszewski, John Wallberg, Sameh Rezeq, Chih-Ming Hung, Oren Eliezer, Sudheer Vemulapalli, Chan Fernando, Ken Maggio, Roman Staszewski, Nathen Barton, Meng-Chang Lee, Patrick Cruise, Mitch Entezari, Khurram Muhammad, Dirk Leipold

Texas Instruments, Dallas, TX

The use of deep-submicron CMOS processes allows for an unprecedented degree of scaling in digital circuitry, but complicates implementation and integration of traditional RF and analog circuits. The explosive growth of cellular radios makes it imperative to find digital architectural solutions to these integration problems. A fully-digital frequency synthesizer and GFSK transmitter for a single-chip Bluetooth radio is proposed in [1]. In this paper, a second generation of the digital radio processor (DRP) targeting GSM/EDGE cellular radios is presented. The all-digital PLL (ADPLL) phase-noise performance is significantly improved through architectural and circuit enhancements, and its wideband frequency modulation capability is extended to accommodate wide frequency deviations for EDGE. To complete the polar TX modulation path, a fully digital amplitude modulation circuit is added.

At the heart of the ADPLL (Fig. 17.5.1) lies a digitally-controlled oscillator (DCO) [2]. The oscillator core (Fig. 17.5.2) operates at twice the 1.6 to 2.0GHz high-band frequency, which is then divided for precise generation of RX quadrature signals. The single DCO is shared between the TX and RX, and is used for both the high bands (HB) and the low bands (LB). Additional 4b of the tracking bank are dedicated for ΔΣ dithering in order to improve frequency resolution. The ADPLL sequencer traverses through the PVT calibration and acquisition modes during channel selection and frequency locking and stays in the tracking mode during the transmission or reception of a burst. To extend the DCO range to accommodate for voltage and temperature drifts, and to allow wide frequency modulation, the coarser-step acquisition bits are engaged by subtracting an equivalent number (generally fractional) of the tracking bank varactors. The acquisition/tracking varactor frequency step calibration is performed in the background with minimal overhead using dedicated hardware. All the varactors are realized as n-poly/n-well MOSCAP devices that operate in the flat regions of their C-V curves. The new varactors and the DCO core structure result in better phase noise than in [2], which is needed to meet the stricter GSM requirements.

The ADPLL operates in the phase domain as follows: The variable phase of the ADPLL is digitally represented by a fixed-point concatenation of the DCO edge-transition count $R_V[k]$ and the normalized time-to-digital converter (TDC) output $\varepsilon[k]$. The TDC measures and quantizes the time differences between the frequency reference (FREF) and the DCO edges. The sampled differentiated variable phase is subtracted from the frequency command word (FCW) by the digital frequency detector. The frequency error $f_E[k]$ samples are accumulated to create the phase error $\phi_E[k]$ samples, which are then filtered by a fourth-order IIR filter and normalized by a proportional loop attenuator α. A parallel feed with coefficient ρ adds an integrated term to create type-II loop characteristics, which suppresses the DCO flicker noise. The IIR filter is a cascade of 4 single-stage filters, each satisfying the following equation: $y[k] = (1-\lambda)\, y[k-1] + \lambda\, x[k]$, where x[k] is the current input, y[k] is the current output, k is the time index, and λ is the configurable coefficient. The 4-pole IIR filter attenuates the reference and TDC quantization noise at an 80dB/dec slope, primarily to meet the GSM spectral mask requirements at 400kHz offset. The phase error samples $\phi_E[k]$ are then multiplied by the f_R/K_{DCO} normalization factor, where f_R is the reference frequency, to make the loop characteristics and modulation independent from the DCO gain K_{DCO}. The modulating data is injected into two points of the ADPLL for the direct frequency modulation [3]. A hitless gear-shifting mechanism for the dynamic loop bandwidth control serves to reduce the settling time. It changes the loop attenuator α several times during the frequency locking while adding the $(\alpha_1/\alpha_2 - 1)\phi_1$ DC offset to the phase error, where indices 1 and 2 stand for before and after the event, respectively. Of course, $\phi_1 = \phi_2$, since the phase is to be continuous.

The ADPLL is a discrete-time sampled system implemented with all digital components connected with all digital signals, allowing the most natural and accurate z-domain representation for it (Fig. 17.5.3).

The pulse-shaping filter of Fig. 17.5.4 contains separate I and Q filters followed by a cordic algorithm to convert to polar-domain phase and amplitude outputs. The sampling rate is 3.25MHz and is interpolated up to 26MHz to further smoothen the modulating signals. The phase is differentiated to fit the FCW frequency format of the ADPLL input. The amplitude output is multiplied by the step size of the digitally-controlled power amplifier (DPA) and is then AM-AM pre-distorted. The amplitude control word (ACW) is then converted to the 64b unit-weighted format of the DPA. A dedicated bank of 8 DPA transistors undergoes a 900MHz 3rd-order ΔΣ modulation to enhance the amplitude resolution and to achieve noise spectral shaping. As in the DCO controller, the DPA controller also performs dynamic element matching (DEM) to enhance the time-averaged linearity. In the GSM mode, a single Gaussian pulse-shaping filter is used and the cordic circuit is bypassed. The AM path is temporarily engaged to ramp the output power to a desired level to remain fixed throughout the payload.

The in-band synthesizer phase noise is measured below –93dBc/Hz for the loop bandwidth of 40kHz (Fig. 17.5.5). The transmitter meets the GSM specifications. The frequency settling time to within the 20Hz GSM phase-slope error is 10μs. Fig. 17.5.6 shows the spectral mask with the corresponding modulated rms phase error of 0.5^0 versus the allowed limit of 5^0. The phase noise at 20MHz offset is –165dBc/Hz, thus, eliminating the need for a SAW filter. The EDGE spectral mask is also met and the rms EVM is below 3.5%, versus the allowed limit of 9%.

Figure 17.5.7 shows a micrograph of the transmitter. It is fabricated in a 90nm digital CMOS process with no analog extensions. At 6dBm output power, the transmitter draws 42mA from a 1.2V supply.

Acknowledgment:
We thank V. Roussel and P. Audinot for system support and E. de-Obaldia and I. Bashir for lab support.

References:
[1] B. Staszewski et al., "All-Digital Phase-Domain TX Frequency Synthesizer for Bluetooth Radios in 0.13μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 272–273, Feb., 2004.
[2] R. B. Staszewski et al., "A First Multigigahertz Digitally Controlled Oscillator for Wireless Applications," *IEEE Trans. Microwave Theory and Techniques*, vol. 51, no. 11, pp. 2154-2164, Nov., 2003.
[3] R. B. Staszewski et al., "All-Digital TX Frequency Synthesizer and Discrete-Time Receiver for Bluetooth Radio in 130nm CMOS Process," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278-2291, Dec., 2004.

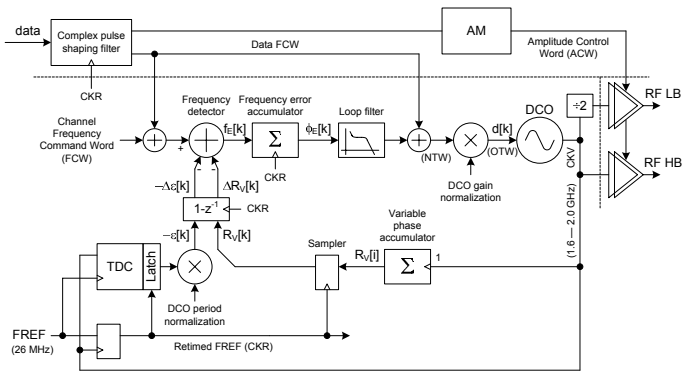

Figure 17.5.1: All-digital PLL (ADPLL) and polar transmitter.

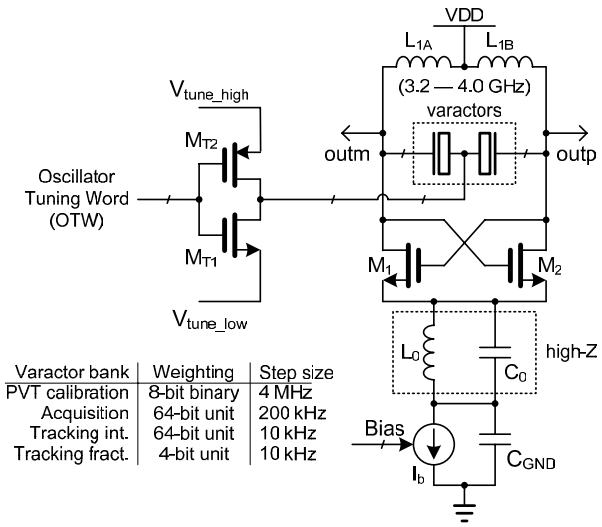

Figure 17.5.2: Digitally-controlled oscillator (DCO) core.

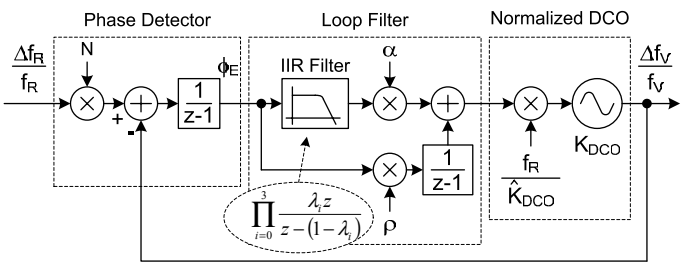

Figure 17.5.3: z-domain model of the ADPLL loop.

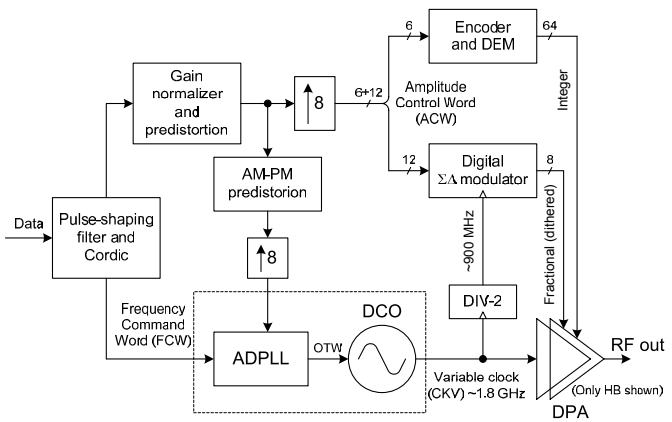

Figure 17.5.4: Amplitude-modulation path of the polar transmitter.

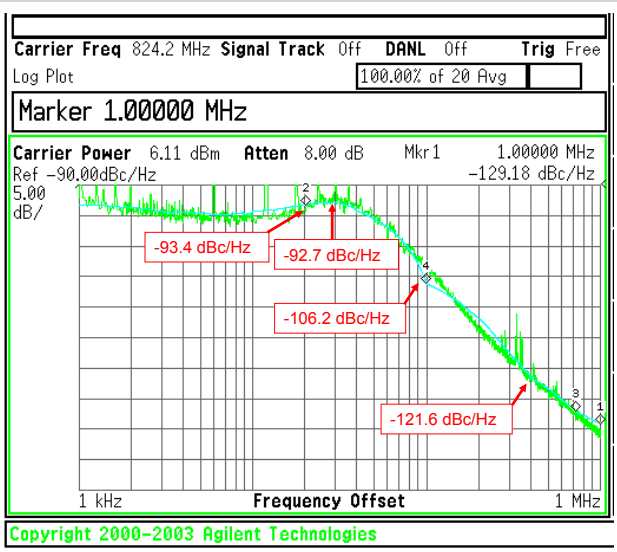

Figure 17.5.5: Phase noise of an unmodulated carrier.

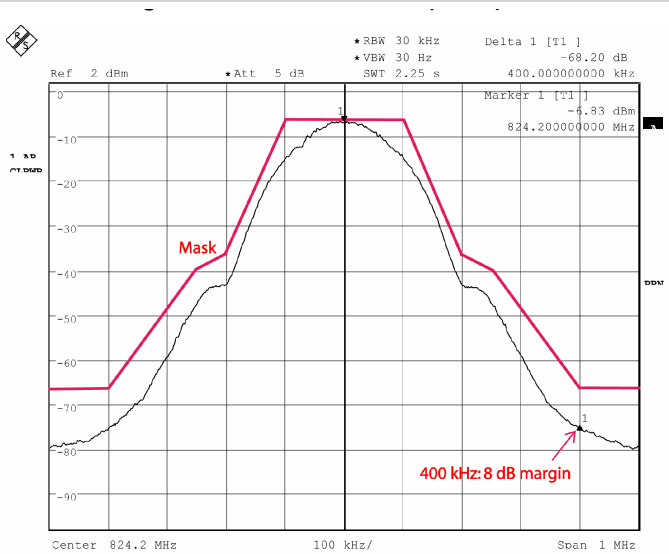

Figure 17.5.6: GSM output spectrum.

Continued on Page 600

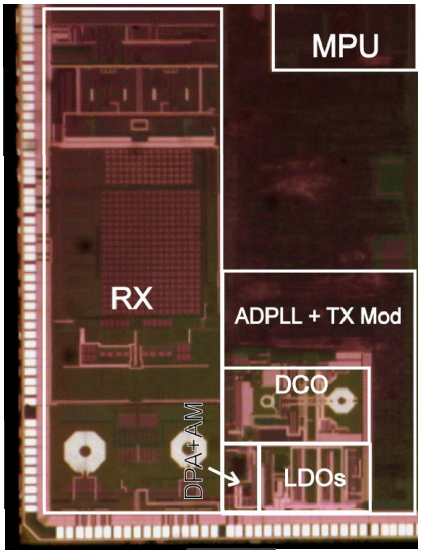

Fig. 17.5.7: Die micrograph.

 0-7803-8904-2/05/$20.00