A 1.8dB NF Receiver front-end for GSM/GPRS in a 90nm Digital CMOS

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Abstract - *An RF receiver front-end for a GSM/GPRS radio system-on-chip in a 90nm digital CMOS technology is presented. The circuit consisting of low noise amplifier, transconductance amplifier, switching mixer and local oscillator, offers 32.5dB dynamic range of gain control that is digitally configurable. Even under the digital spurious noise, the noise figure in the 40dB maximum gain is 1.8dB and +50dBm IIP_2 in 34dB gain. The variation of the input matching versus multiple gains is less than 1dB. The local oscillator to drive the mixer fulfills the stringent phase noise requirement of -153.5 dBc/Hz at 3-MHz. The circuit occupies 1.62mm^2. The LNA, TA and mixer consume less than 15.3mA at a supply voltage of 1.4V.*

Keywords: radio frequency, low noise amplifier, receiver front-end, transconductance amplifier, mixer, digitally controlled oscillator.

1 Introduction

The continuous scaling in CMOS technology allows higher level of integration resulting in lower solution price while offering more features and functionalities. Designing a radio for the GSM/GPRS standard with large digital circuits offering PHY and MAC layers on the same chip becomes a challenging task due to the coupling of the digital spurious noise through silicon substrate, interconnect and package. While high level of integration impedes achieving a low noise figure, low supply voltage makes linearity hard to achieve.

Recently, we demonstrated a highly integrated system-on-chip (SOC) in the discrete-time Bluetooth receiver [1]. In this paper, we present an RF receiver front-end in a 90nm digital CMOS process having an embedded variable gain amplifier (VGA) function that is digitally configurable and offers fine gain control. The S_{11} is constant over the desired frequency range while achieving 1.8dB NF in the highest gain setting of 40dB with 15.3mA. The gain can be configured with an automatic-gain-control algorithm to select an optimal setting with a trade-off between noise figure and linearity and to compensate the process and temperature variations. The objective is to realize a receiver front-end circuit that is small in size while enabling the software-defined radio (SDR) of the future.

2 Architecture

The receiver front-end is shown in Figure 1 and consists of an LNA followed by two transconductance amplifiers (TAs) and two passive mixers. The RF input signal is amplified by the LNA and splits into I/Q paths where it is further amplified in the TA. It is then down-converted to a low intermediate frequency (IF) that is fully programmable (but defaults to 100kHz) by the following mixers driven by an integrated local oscillator (LO). The LO signals are generated using an all-digital PLL (ADPLL) [2] that incorporates a digitally-controlled oscillator (DCO). Although the front-end circuit requires two TAs, two mixers and quadrature LO signals, the receiver has an excellent sensitivity and good linearity at a low supply voltage (V_{DD}) of 1.4V thus offering excellent performance that satisfies GSM requirements. The power is supplied by an integrated low-drop-out (LDO) regulator.

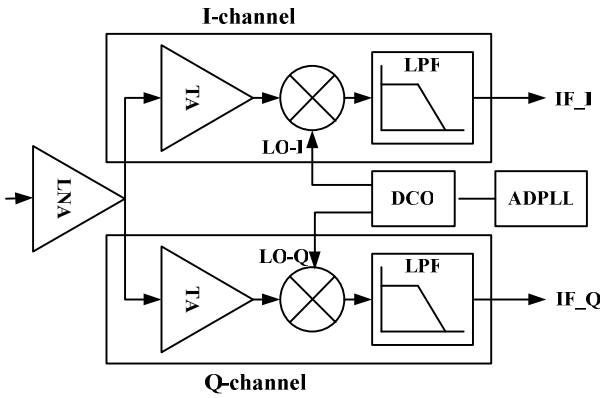

Figure 1. Receiver front-end diagram

2.1 Low Noise Amplifier

Figure 2 shows a simplified schematic diagram of the LNA. A differential LNA is implemented to improve noise figure from substrate coupling originated from digital base-band circuits since the impact of the switching noise of more than a million digital gates on the same substrate was not known. A variable gain feature with seven digitally configurable steps is implemented. In the high gain mode, four voltage gains are realized with a 2dB step between 21dB and 29dB. In the low gain mode, there are

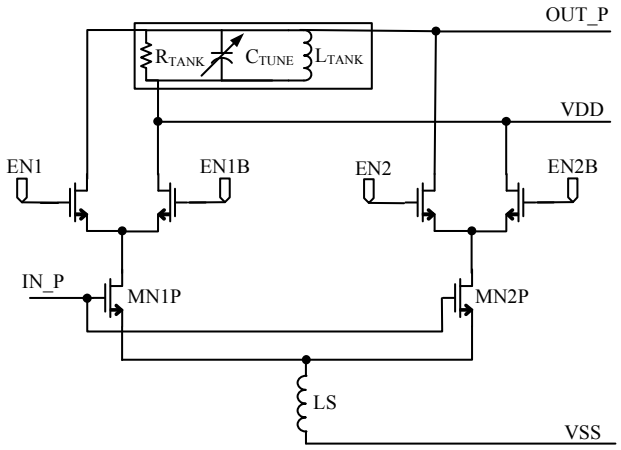

Figure 2. LNA core schematic

three gain steps with a 2dB step between 3dB and 9dB. As shown in Figure 2, the multiple cascode stages are connected in parallel with one source degeneration inductor (L_S) and one inductive load. Each stage has two branches for digital configurability.

The top transistors of the cascode stage used for bypassing gain contribution are shunted to V_{DD}. Since the bottom transistors of the cascode stage operate in all gain settings, to the first order the input impedance is constant over gain selections which is critical for constant input power and noise matching. Inductive source degeneration using package bond wires is implemented to improve linearity. The LNA load is an on-chip spiral inductor using multiple metal layers with metal width=5.9μm, metal space=2μm, inner diameter=81.9μm and 10 turns. This inductor is drawn as a center-tap configuration for better matching between the differential branches and achieving a higher quality factor (Q). The inductance is 8.9nH and Q is > 4 at 900MHz, where Q is defined as $|\text{imag}(y_{11})/\text{real}(y_{11})|$. To reduce the substrate effect, all doping under the inductor is blocked to preserve a higher resistivity.

The inductor is tuned with the capacitance at the LNA load which comprises tuning capacitors together with parasitics. The tuning capacitor is realized using Metal-Insulator-Metal (MIM) capacitors and switches. As shown in Figure 3, two capacitors are connected differentially with a switch and two pull-down transistors to keep both source/drain voltages of the switch low and Q of the capacitor bank high. The achieved effective Q is 100 at 900MHz. When the switch is turned off to be in a low capacitance value, the parasitic capacitance of the MIM capacitors and transistors still has an effective Q of ~100. Compared to MOS capacitor, MIM capacitor provides a much better trade-off between Q and C_{ON}/C_{OFF} ratio. In this design, a C_{ON}/C_{OFF} ratio of larger than 4 was achieved while Q is still greater than 100. The selectable capacitance ranges 2.5pF in total because in this process, MIM capacitance can vary up to +/-20% from its nominal value. With this design, all GSM bands can be fully covered.

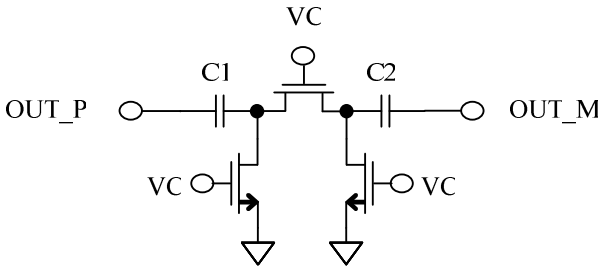

Figure 3. Tuning capacitor schematic

The differential LNA draws 7.3mA. The LNA input is protected against ESD by one reverse-biased diode to V_{DD} and three forward-biased diodes in series to V_{SS}. ESD structures at LNA input are aimed to protect larger than 2KV HBM. The LNA bond pad is shielded with lower metal-1 layer to eliminate the substrate coupling while minimizing parasitic capacitance which is about 100fF.

2.2 TA and Mixer

Figure 4 shows a simplified TA and mixer schematic diagram. A highly efficient push-pull amplifier is chosen for the TA because of its low noise and good linearity characteristics. The variable gain feature is implemented in the TA with a 3-bit control. A feedback amplifier is used to set the dc bias voltage of the TA output node to V_{REF} which is set to half of V_{DD} so as to provide maximum signal swing. Resistors in Figure 4 are large enough to prevent significant RF signal loading. The differential TA draws 4mA in the maximum gain mode.

A double-balanced switching mixer is connected to the TA output via ac-coupling capacitors so that the dc voltage at the TA output is isolated from the mixer. This topology has an excellent feature of reduced 1/f noise because there is no dc current flowing through the mixer switches, making it suitable for direct-conversion or near-zero IF receivers. By adding a capacitive load (C_H, history capacitor) to the mixer output, low pass filtering can be obtained to reduce large interferers. In this mixer, two switches are toggled by one of the out-of-phase LO signals (LO+, LO-) from a digitally-controlled oscillator (DCO). Since the mixer is connected to a subsequent circuit like

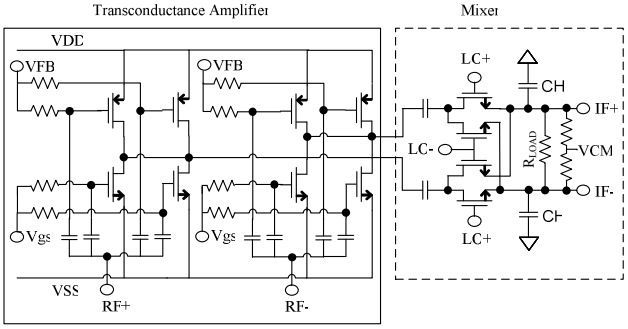

Figure 4. TA and Mixer core schematic

an analog-base-band circuit, R_{LOAD} represents the loading effect, which is about 4.5KΩ.

2.3 DCO

A DCO circuit schematic is shown in Figure 5 [3]. L_{1A} and L_{1B} are two halves of a center-tap inductor. Because of the short-coming of this 90nm digital CMOS Cu process which has thin metal interconnects, it is difficult to design an inductor with even a moderate Q. To enhance the Q of the inductor, an Al layer is patterned and connected in parallel with the Cu windings. M3-5 plus the Al layer were used to form L_1 while only M3-5 layers were used for L_0. The total Cu and Al thickness are only 0.75μm and 1.0μm, respectively. The simulated single-ended Q using an imag(y_{11})/real(y_{11}) definition is 3.6 and 6.7 at 0.9 and 3.6 GHz, respectively. The differential phase-stability Q is 3.6 and 10.2 at 0.9 and 3.6 GHz, respectively [4].

The varactor is implemented using an npoly-nwell MOSCAP structure. Extrapolating from measurement data, the C_{max}/C_{min} ratio is > 3 within the ranges of desired gate length L_g and gate width W_g per finger. The resulting total tolerable fixed parasitic capacitance is 720 fF. MOSCAP was chosen because the gate oxide thickness (t_{ox}) is one of the best controlled parameters in this CMOS process, whose corner variation is within +/-2.5%. The four different phases of LO driving the I- and Q-mixers in Figure 4 are generated from the DCO frequency which oscillates at $4\omega_0$, where ω_0 is in the GSM band frequencies. A fully digital circuit (ADPLL) is built around the DCO to adjust its phase and frequency deviations in a negative feedback manner.

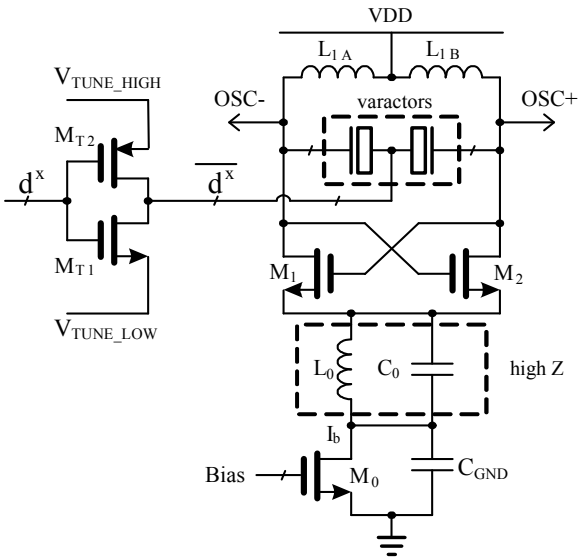

Figure 5. DCO core schematic

3 Performance

The LNA input is matched using external inductor and capacitor with a balun for impedance transformation from 50 to 100Ω. Figure 6 shows the measured LNA input matching with $|S_{11}|$ <-10dB over the whole GSM band. The measured curves of S_{11} versus multiple LNA gains are displayed and compared, where maximum variation is less than 1dB. Figure 7 displays the front-end voltage gains versus different LNA and TA gain settings. The front-end gains can be configured with an automatic-gain-control (AGC) function to select an optimal gain setting trading off noise figure for linearity. This circuit adds 32.5dB dynamic range to the receiver. The measured noise figure in the maximum gain mode is 1.8dB which is excellent, when considering the fact that several hundred thousand digital logic gates are switching on the same substrate.

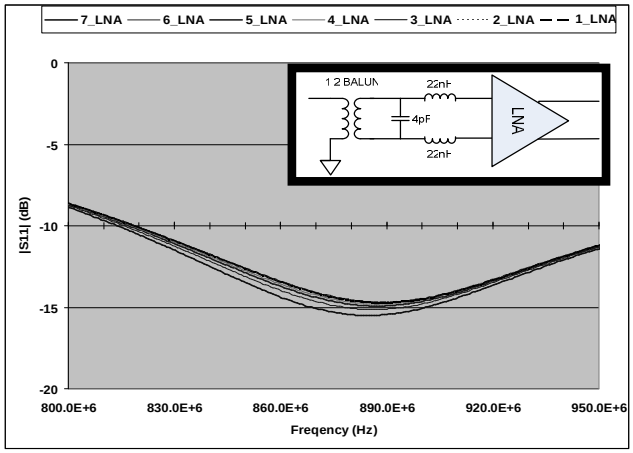

Figure 6. Measured S_{11} in LNA gains

With LO frequency set to 869.1MHz, +50dBm of IIP_2 is measured with a front-end gain of 34dB where the LNA gain is set to 2dB below the maximum gain (6_LNA) and TA to its middle gain setting (3_TA). To mimic the EDGE environment, two tones of 875.2MHz and 875.3MHz are injected into the LNA for the IIP_2 test (power of -36dBm).

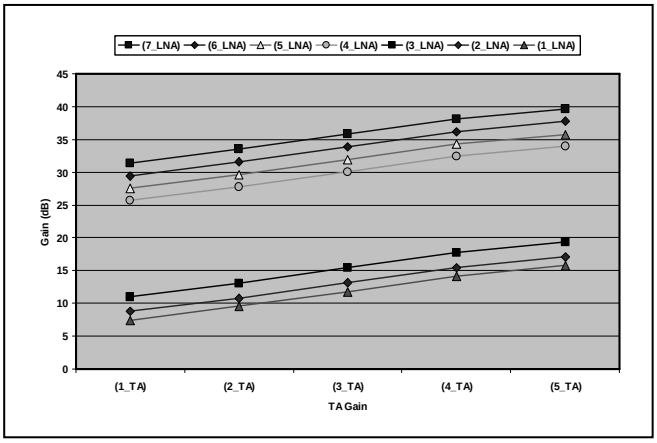

Figure 7. Measured voltage gain

The LNA, two TA's and mixers consume 15.3mA from an internal LDO voltage of 1.4V. Since this work has digitally configurable gain with a fine resolution, it is different from a conventional front-end approach that is typically built for two large steps. A major advantage of our approach is that the circuit performance can be finely optimized by selecting the appropriate gain settings. Table-I summarizes the measured performance when the front-end gain of 34dB is selected with LNA gain setting number 6 (max-2dB) and TA gain setting number 3.

The phase noise of the DCO is plotted in Figure 8 for the signal power level of 5.8dBm. The phase noise at 600-kHz, 3-MHz and 20-MHz offsets are -136.8, -153.5 and -166.9dBc/Hz, respectively from the dynamic frequency divider output. The DCO and the dynamic divider consume 12 and 2 mA, respectively from 1.4V supply.

Table I. Measured performance

	Measured Data
Noise figure (1K ~ 100KHz)	2.0 dB
NF with -25dBm blocker at 3-MHz offset	5.0 dB
S_{11}	< -10 dB
IIP_2	+50 dBm
IIP_3	-15 dBm
P_{1dB}	-25 dBm
Gain	+34 dB
Front-end current consumption	15.3 mA

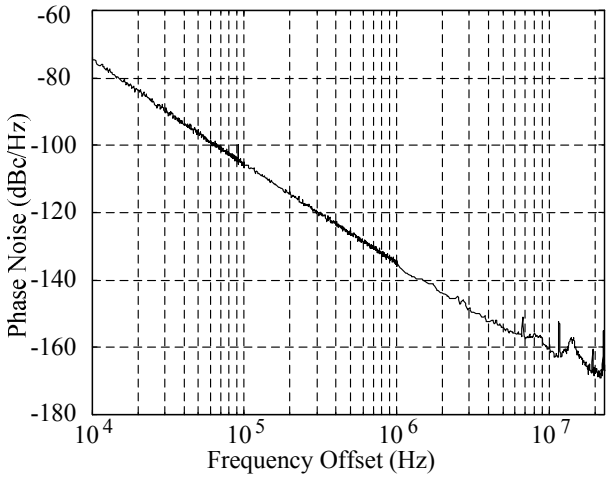

Figure 8. Measured DCO phase noise

The chip has been fabricated in a 90nm digital CMOS process with copper interconnects, 0.27µm minimum metal pitch, 2.8nm gate oxide thickness and no extra processing steps for analog functions. It is housed in a conventional BGA package. The die-micrograph showing GSM radio front end is shown in Figure 9 and it occupies 1.62mm^2.

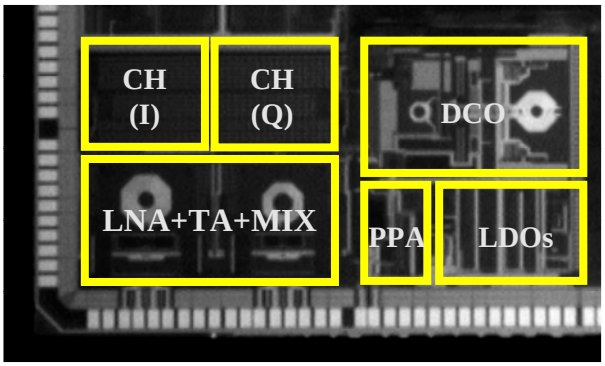

Figure 9. Die photo of GSM receiver front-end

4 Conclusions

A GSM receiver front-end including LNA, TA, Mixer for I and Q channels with low-pass-filter capacitor and DCO is presented. It is implemented for a fully integrated GSM/GPRS radio using a 90nm digital CMOS technology. While providing 35 digitally-configurable voltage gain steps ranging from 40dB down to 7.5dB, this fully integrated front-end circuit demonstrates a good noise figure of 1.8dB at 40dB maximum gain and +50dBm IIP_2 at 34dB of gain, while a million of digital logic gates are simultaneously running on the same substrate. This receiver front-end demonstrates a cellular radio design using the state-of-the-art digital CMOS processes and further proves the feasibility of implementing multiple radios with digital configurability in a single chip.

5 Acknowledgement

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