RF Amplitude Control in an All-Digital PLL based Transmitter

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***Abstract*— A fully-digital frequency synthesizer for RF wireless applications has recently been proposed. At its foundation lies a digitally-controlled oscillator that deliberately avoids any analog tuning controls. The conventional phase/frequency detector, charge pump and RC loop filter are replaced by a time-to-digital converter and a simple digital loop filter. When implemented in a digital deep-submicron CMOS process, the proposed architecture is more advantageous over conventional charge-pump-based PLL's since it exploits signal processing capabilities of digital circuits and avoids relying on the fine voltage resolution of analog circuits. In this paper, we present new techniques for achieving amplitude control of the RF output. This approach has been incorporated in a Bluetooth radio realized in 130-nm CMOS.**

I. Introduction

With the explosive growth of the wireless communications industry worldwide, the need has arisen to reduce cost and power consumption of mobile stations. The use of deep-submicron CMOS processes allows for an unprecedented degree of scaling and integration in digital circuitry, but complicates the implementation of traditional RF and analog circuits. Consequently, a needed has arisen to find digital architectural solutions to the RF functions.

RF frequency synthesizer is a key block used for both up-conversion and down-conversion of radio signals. It has been traditionally based on a charge-pump PLL, which is not easily amenable to integration and suffers from high level of reference spurs generated by the correlative phase detection method. Recently, a *digitally-controlled oscillator* (DCO), which deliberately avoids any analog tuning voltage controls, was proposed and demonstrated in [1] for RF wireless applications. This allows for its loop control circuitry to be implemented in a fully digital manner as first proposed in [2] and then demonstrated as a novel digital-synchronous phase-domain *all-digital* PLL (ADPLL) in a 130 nm CMOS single-chip Bluetooth radio [3]. The phase-domain operation does not fundamentally generate any reference spurs thus allowing for the loop filter to be set at an optimal point between the reference phase noise and oscillator phase noise.

An important issue in today's wireless transmitters is the efficient regulation of the output power. This paper presents novel techniques used within the framework of the ADPLL to regulate the RF output amplitude for the purpose of the power control requirements of the wireless standard. The technique could be extended for the dynamic envelope control of the phase-modulated digital carrier.

II. All-Digital PLL Operation

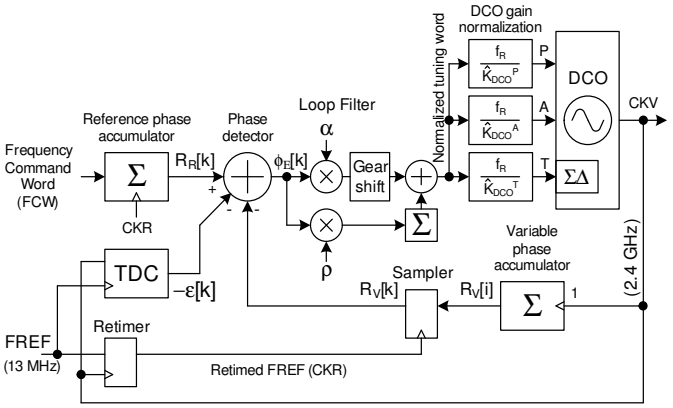

Fig. 1. Block diagram of the all-digital PLL.

Fig. 1 shows an ADPLL-based frequency synthesizer. The output *variable frequency* (f_V) is related to the *reference frequency* (f_R) by the frequency command word $FCW = f_V/f_R$. The ADPLL operates in the phase domain [3] as follows. The variable phase $R_V[i]$ is determined by counting the number of rising clock transitions of the DCO oscillator clock CKV: $R_V[i] = \sum_{l=0}^{i} 1$. The index i indicates the DCO edge activity. The reference phase $R_R[k]$ is obtained by accumulating FCW with every cycle of the retimed *frequency reference* (FREF) clock input operating at f_R: $R_R[k] = \sum_{l=0}^{k} FCW[k]$. The FREF-sampled variable phase $R_V[k]$ is subtracted from the reference phase $R_R[k]$ in a synchronous arithmetic phase detector producing phase error samples: $\phi_E[k] = R_R[k] - R_V[k] + \varepsilon[k]$. The FREF retiming quantization error $\varepsilon[k]$ is determined by the *time-to-digital converter* (TDC). The TDC is built as a simple array of inverter-delay elements and flip-flops, which produces a time conversion resolution finer than 40 ps in this 130 nm process.

The digital phase error $\phi_E[k]$ is attenuated by the loop gain factor α and then normalized by the DCO gain K_{DCO} in order to correct the DCO phase/frequency in a negative feedback manner with the loop dynamics that are independent from variations in the manufacturing process, in the supply voltage and in the operating temperature. The phase error attenuator factor α establishes the PLL loop first-order filtering characteristic:

$$f_{BW} = \frac{\alpha \cdot f_R}{2\pi} \quad (1)$$

where f_{BW} is a 3-dB cut-off frequency of the closed PLL loop. The α value is changed several times during the frequency locking with an initial $\alpha = 2^{-3}$ and final $\alpha = 2^{-8}$ values resulting in $f_{BW} = 259$ kHz and $f_{BW} = 8$ kHz, respectively, for f_R = 13 MHz reference frequency. The final value of α was chosen to be the best tradeoff between the phase noise of the reference input and the DCO phase noise during the TX and RX operations. The integral loop factor $\varrho = 2^{-18}$ is activated shortly after the loop is settled. It switches the PLL characteristic from type-I to type-II with the damping factor $\zeta = \frac{1}{2}(\alpha/\sqrt{\varrho}) = 1$ in order to effectively filter out the oscillator flicker noise, which is typically quite high in a deep-submicron CMOS.

With $W_F = 15$ fractional part wordlength of the fixed point $R_R[k]$ accumulator, the ADPLL provides fine frequency control with 400 Hz accuracy, according to $\Delta f = f_R/2^{W_F}$. The number of integer bits $W_I = 8$ was chosen to fully cover the Bluetooth frequency range of f_V = 2400–2480 MHz.

III. Power Amplifier

This section deals with the last stage on the integrated transmitter path – power amplifier (PA). The purpose of a PA in a Bluetooth system is to deliver several mW of RF power to the antenna in an efficient manner. In a GSM system, this block would serve as a *pre-power amplifier* (pre-PA or PPA) delivering several mW of RF power to an external PA with an output on the order of a watt.

Power amplifiers have been traditionally categorized under many classes: A, B, C, D, E and F [4]. Classes A, B and C are considered classical in the sense that both the input and output waveforms are sinusoidal. Voiding this assumption with class E and F operation leads to higher performance and efficiency.

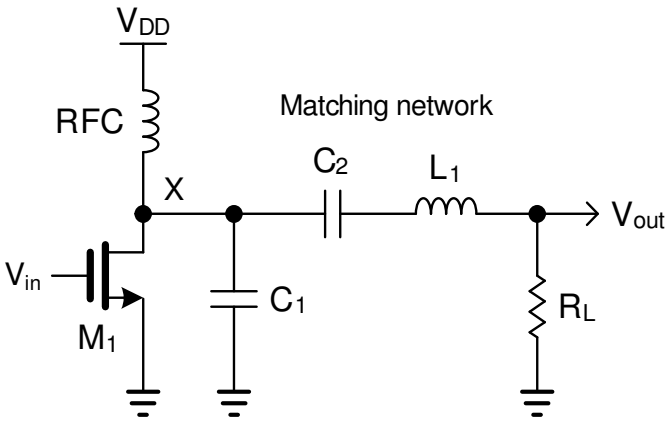

Fig. 2. Class-E power amplifier.

Class-E stage is a nonlinear amplifier that potentially achieves 100% efficiency while delivering full power. It has been shown to be best suited in a low-voltage environment [5]. An ideal schematic is shown in Fig. 2. Transistor M_1 is used here as an on/off switch. RFC is a radio-frequency choke, a large external inductor (usually about 100 nH) that acts as a bi-directional current source at RF frequencies, and which connects the switch to the supply voltage V_{DD}. C_1 is a capacitance connected in parallel to the switch and includes the parasitic capacitance of M_1. The C_2-L_1 filter circuit is tuned to the first harmonic of the input frequency and only passes a sinusoidal current to the load R_L.

The values of C_1, C_2, L_1 and R_L are chosen such that V_X is close to satisfying three conditions [4]:

1) As the switch turns off, voltage on X, V_X, remains low long enough for the current to drop to zero.
2) V_X reaches zero just before the switch turns on.
3) dV_X/dt is near zero when the switch turns on

In this case, as almost universally in GHz-range applications, the load resistance R_L is 50 Ω. Inductor L_1 is realized as a bond-wire of a 3 nH value. C_2 is an external 1.5 pF capacitor. C_1 is an internal metal-to-metal 1.4 pF capacitor. The M_1 transistor is a 32-finger NMOS of size W/L = 2.5/0.15.

During the time when the switch is closed, the voltage across it is close to zero. During the time when the switch is open, the current through it is close to zero. Since the voltage and current of the switch do not overlap, the power dissipation of the switch is ideally zero. When the switch turns off, the current through RFC splits between the two branches containing C_1 and R_L. The capacitance C_1 starts charging and produces a voltage across the switch with peak of up to 2xV_{DD}. Satisfying condition (1) is quite easy and it is guaranteed by C_1. Without C_1, V_X could rise as V_{in} is dropped introducing substantial power loss in M_1. When the switch turns on, any charge stored on C_1 will be discharged to the ground resulting in a power loss. In order to avoid this, the circuit must be designed to satisfy conditions (2) and (3) such that the voltage across M_1 reaches zero at the turn-on time and stays there for some time.

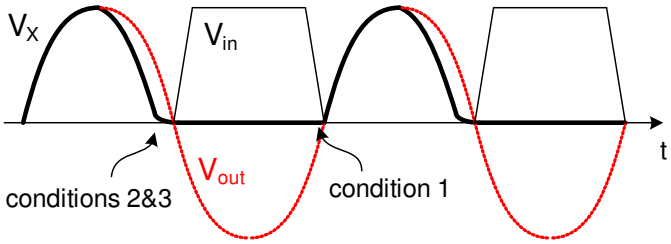

Fig. 3. Waveforms of the class-E PA.

After the switch turns off, the load network operates as a damped second-order system with overdamped, underdamped or critically damped response. If the quality factor Q of the network makes it critically damped, then the drain voltage of M_1 will follow the V_X curve in Fig. 3. This will satisfy conditions (2) and (3). If the network response is underdamped, there would be a dying oscillatory response of V_X and condition (3) could not be met. If the network response is overdamped, V_X might not reach zero by the time M_1 turns on. It should be noted that due to the inverting nature of the amplifier, the input and output waveforms are shifted by 180 degrees.

In the ideal situation mentioned above, the efficiency of a class-E amplifier is 100%. However, in practice, the switch

has a finite on-resistance, and the transition times from the off-state to the on-state and vice-versa are not negligible. Both of these factors result in power dissipation in the switch and reduce efficiency [5].

The class-E power amplifier was chosen in the proposed architecture due to the following reasons:

- Low voltage operation – ideally suited for deep-submicron CMOS. The end stage transistor operates as a switch. Unlike in class A, B and C stages where the transistor acts as a current source and the V_{ds} must be precisely controlled at all times to be high enough in order to avoid entering the triode region, the V_{ds} here can be arbitrarily low and no control is necessary. The only requirement is that the V_{gs} must be able to go higher than the threshold voltage for the transistor to turn on.
- Digital input – the transistor switch works best with digital input waveforms, preferably with sharp rise and fall times. Contrast it with the classical PA's which require sinusoidal inputs. This is where the deep-submicron strengths lie. The DCO output is already in a digital format. Duty cycle of the input waveform can conveniently control the output amplitude and power.
- Class-E stage is preferred over class-F, which is similar to class-E but has an additional filtering network to create a high impedance load at the transistor drain for the second or third harmonics, thus sharpening the edges. The filtering network requires an extra LC tank, which is quite area-expensive in a deep-submicron process. In addition, class-F amplifiers have consistently shown in practice worse performance than class-E amplifiers [5].
- High power efficiency: theoretically 100%, but in practice 80-90% have consistently been reported [5]. The efficiency does not degrade substantially with the output power.

Since the targeted output power for Bluetooth or GSM (pre-PA) applications is only several mW, the efficiency is not as important as meeting the basic design specifications, which in itself is quite a challenge at 1.5 V supply. In this case, it is still advantageous to operate the power amplifier with a digital switch, even though the class-E conditions might not be fully met.

IV. Digital Amplitude Modulation

As mentioned in Sec. III, the output power of a class-E RF power amplifier could be controlled by changing the duty cycle or pulse width of its RF digital input. The pulse width controls how long the switch is turned on during the RF cycle and, consequently, how much energy gets transferred to the load R_L. This idea, shown in Fig. 4, is proposed to be used for the transmitted RF amplitude and power control. In the implemented Bluetooth testchip, only a static RF power control is required and this is here accomplished through the RF waveform amplitude control.

As of this writing, there have been no reports on using this kind of pulsewidth modulation in RF applications. A well-known reference [6] states that this idea is "fairly useless at

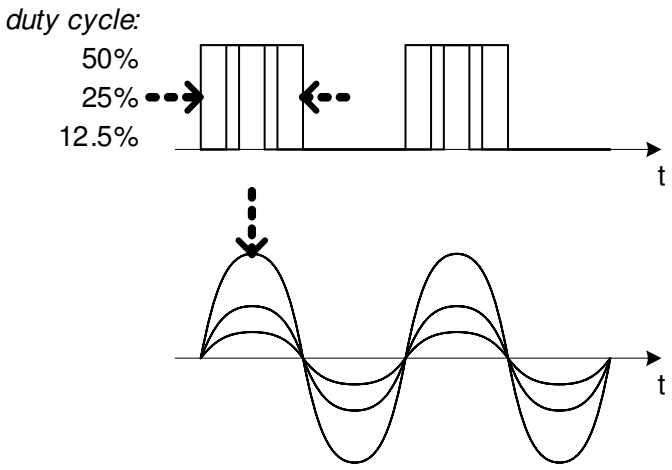

Fig. 4. Output power control through duty cycle of the class-E PA input.

the gigahertz carrier frequencies of cellular telephones. (...) difficult to use pulsewidth modulation once carrier frequencies exceed roughly 10 MHz." This research successfully achieved the 2.4 GHz operation, mainly due to the ultra-fast speed of operation of digital logic gates in this modern deep-submicron process.

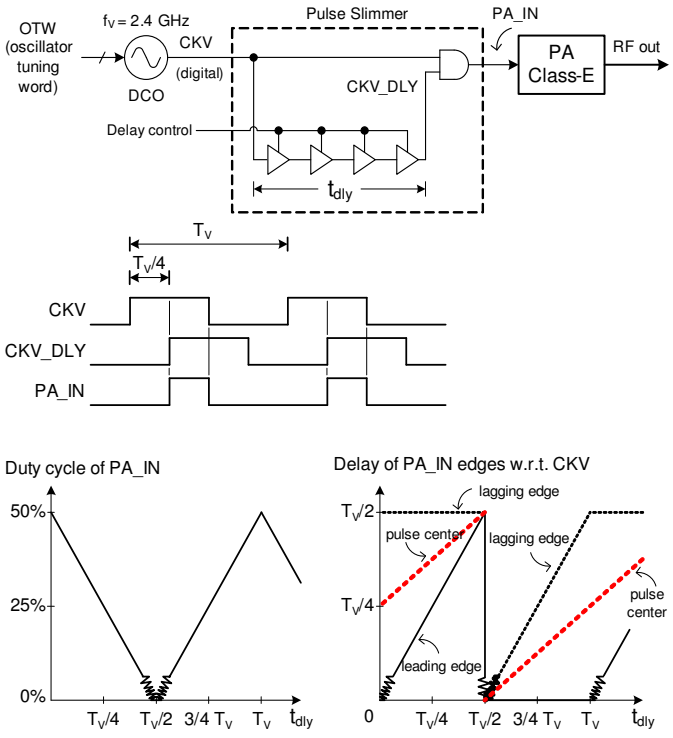

Fig. 5. Digital amplitude control through pulse-width modulation.

Fig. 5 shows an example implementation of an amplitude modulation using a digital pulse slimmer method. The digital oscillator output clock CKV is met at the digital AND gate with its delayed replica. The delay path could be constructed of a string of inverters or buffers, in which the delay could

be controlled through a current-starving mechanism or variable capacitative load. In this implementation, delay control through a variable power supply voltage was chosen. The AND gate output is connected to a class-E power amplifier input PA_IN. Depending on the relative time delay of the two paths, the timing and duty cycle of the AND gate output could be controlled. The duty cycle or pulse-width variation directly affects the turn-on time of the PA digital switch, thus establishing the RF output amplitude. The amplitude-vs.-pulsewidth relationship is quite linear, except for the very narrow input pulse which might not have enough energy to reliably turn on the switch. This non-linear region of operation could descriptively be called a "dead zone" – a reference to a commonly used term in conventional phase detectors. The dead zone could be entirely avoided at a system level by choosing modulation techniques that guarantee a certain minimum level of the signal envelope. For example, GFSK and GMSK are *constant*-envelope modulation schemes. Offset-8PSK is a modulation technique used in GSM-EDGE that purposefully rotates the I-Q constellation with every symbol so as to avoid the origin. These methods have been employed for a long time to improve efficiency of power amplifiers and to facilitate the use of a saturation mode of operation.

The timing diagram on the bottom right of Fig. 5 shows two regions of operation with different behavior of leading and lagging output edges with respect to the t_{dly} delay of the delay path. In the first region, the leading edge of the output traverses but the lagging edge does not. A reversed operation takes place in the second region (dotted line). Since the pulse position is determined of where its center lies, neither of the two provide orthogonality of the phase modulation in the oscillator and the amplitude modulation in the oscillator pulse slimmer circuit. Consequently, the phase adjustment is necessary with the amplitude change. This is not a difficult task since the phase control is in the digital domain through manipulation of the *oscillator tuning word* (OTW).

In order to save power and reduce jitter due to the long chain of buffers or inverters in the delay path, it might sometimes be beneficial to use an inverted CKV_DLY signal, which is equivalent to an extra half-cycle ($T_V/2$) periodic shift. This could be accomplished through either feeding the delay path from the inverted CKV clock output, or inverting the CKV_DLY signal itself. It is important to note that the maximum required amount of delay is never greater than half of the CKV clock cycle since the negated CKV (of the opposite phase) could always be used.

V. Implementation and Results

Fig. 6 shows a die micrograph of a complete single-chip Bluetooth radio that contains the 2.4 GHz ADPLL-based frequency synthesizer and transmitter. It is fabricated in a 130 nm digital CMOS process. Total continuous power consumption during TX is only 38 mA at 1.5 V supply and 4 dBm RF output power.

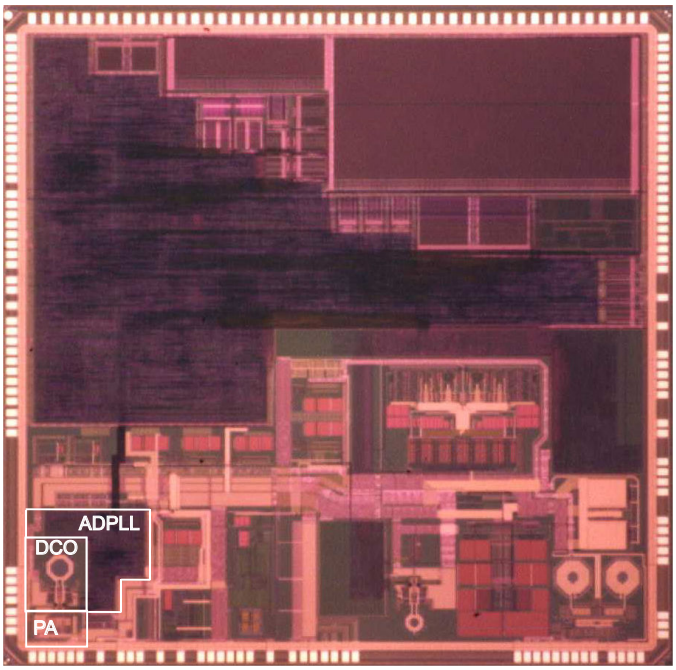

Fig. 6. Die micrograph of the single-chip Bluetooth radio.

VI. Conclusion

We have proposed a new approach for achieving an amplitude control of an RF carrier in a wireless transmitter. This technique feeds the digital clock output of an RF digitally-controlled oscillator into a pulse slimmer that adjusts the pulse-width of its output. The signal is then supplied to a class-E power amplifier that produces the RF carrier with a amplitude level proportional to the input pulse width. In Bluetooth, the method allows for a regulation of the output power. When combined with the direct all-digital phase modulation, the method allows for an implementation of a polar transmitter. The presented ideas have been incorporated in a single chip Bluetooth radio realized in 130-nm CMOS.

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