A Highly Selective, Very Linear Low Noise Transconductance Amplifier Capable of Large-Signal Handling for Current-Mode Receivers Front-End

Master of Science Thesis

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by

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ABSTRACT

The staggering advances in mobile phone industry and wireless technologies have led to abundance of wireless and cellular standards over the past few years. Most of the emerging radio standards (such as 4G LTE and WiMax) require flexible RF transceivers capable of handling various bandwidths and modulation scheme. Meanwhile, the demand by manufacturers for miniaturization, power and cost reduction have compelled further integration of RF transceivers by juxtaposing multiple RF SoC cores on a single silicon die. The prominent challenge in multi-radio chips is blocker interference. Blocker constraint in cellular radios is very stringent, requiring external SAW filters or high performance duplexers. However, SAW filters are bulky and expensive; plus, they reduce the receiver flexibility and degrade the RX sensitivity by a few dB. To circumvent these issues, "true SAW-less" receivers (by removing the SAW filter at the input of the RX) have been proposed in the literature. To achieve the ultimate flexible and multi-core radio operation, wide-band RX RF front-ends robust against interference, in excess of the requirements usually specified by a radio standard, are required.

In this work, a highly selective, very linear LNTA capable of large-signal handling for current-mode RX front-ends is proposed and implemented in 65-nm CMOS technology. It is shown that by combining the on-chip high-Q bandpass filters with a push/pull class-AB common-gate stage, a large desensitization point (B_{1dB}) and large-signal IIP3 of +8 dBm and +20 dBm, respectively, can be achieved, with 1.5 V supply voltages and 7.5 mA current consumption. Meanwhile, by applying noise cancellation technique, via an auxiliary push/pull class-AB common-source stage, a moderate NF of 5.9 dB is possible, which is a very competitive number for such value of B_{1dB}.

ACKNOWLEDGMENTS

And yet another chapter in my life has faded away, and it has taught me a precious little lesson:

"Patience is bitter, but its fruit is sweet."

Foremost, I would like to express my sincere gratitude to my supervisor Prof. Robert Bogdan Staszewski, whose kindness, patience, enthusiasm, and astuteness, as well as his experience, have been invaluable to me during this project.

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Last but not the least, a very special thank to my sweetheart Bahar for her love, tremendous support, and endurance during this study. She has filled my life with joy and splendid memories. I would like to dedicate this thesis to her, whose love is worth it all.

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INTRODUCTION

1.1 Towards Multi-band, Multi-radio Coexistence

The abundance of wireless and cellular communication standards has made the incorporation of multi-band, multi-mode radios into mobile devices a pervasive trend. Along with 2G/3G/4G radio access technologies, a modern mobile platform usually needs to handle other connectivity standards such as Wi-Fi or Bluetooth. An example combination of various modes in a modern mobile platform is shown in Figure 1.1 [1]. Moreover, the number of bands to be supported by the emerging radio standards, such as LTE or WiMAX, has increased explosively [2], [3].

Numerous applications such as smartphones, PDAs, tablet PCs, and game consoles require multi-mode, multi-band operation. Due to the lucrative and booming market of mobile devices (smartphones, alone, have a $219 billion market value[1]), substantial investments have been done in both academia and industry to develop and improve the essential components used in them such as RF transceivers, memory, power management units, etc.

Nowadays, manufacturers have already accomplished to incorporate multi-mode, multi-band operation into existing mobile devices, especially smartphones. In Table 1.1, four popular

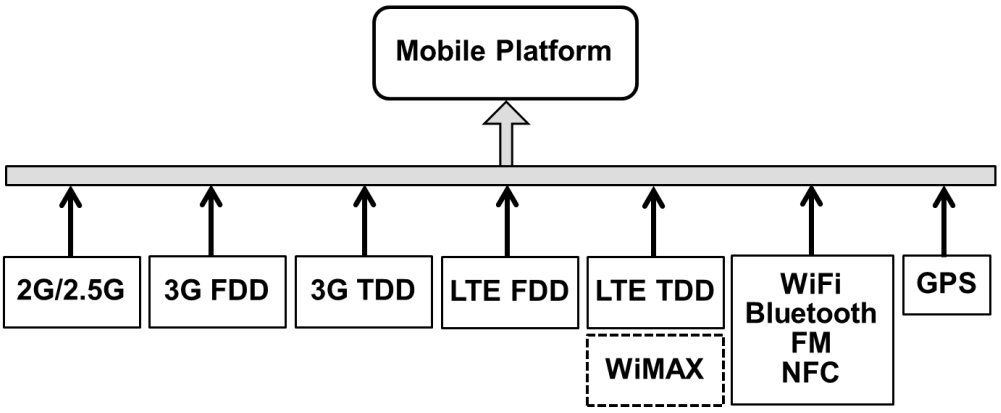


Figure 1.1: Multi-mode scheme for modern mobile platforms [1].

[1] *http://www.bloomberg.com/news/2012-10-17/smartphones-in-use-surpass-1-billion-will-double-by-2015.html*

Model	iPhone 3GS	iPhone 4S	iPhone 5 (Model A1429)	Samsung Galaxy S III
Year	2009	2011	2012	2012
Supported Connectivity	-Quad-band GSM/GPRS/EDGE -Tri-band UMTS/HSDPA (Bands I,II,V) -WLAN (802.11b/g) -Bluetooth 2.1 -GPS	-Quad-band GSM/GPRS/EDGE -Quad-band UMTS/HSDPA /HSUPA (Bands I,II,V,VI) -CDMA EV-DO Rev. A (800/1900 MHz) -WLAN 2.4GHz (802.11b/g/n) -Bluetooth 4 -Assisted GPS -GLONASS	-Quad-band GSM/GPRS/EDGE -UMTS/HSPA+/DC-HSDPA (Bands I,II,V,VI) -CDMA EV-DO Rev.A and B (800,1900, 2100 MHz) -LTE (Bands 1,3,5,13,25) -WLAN 2.4GHz and 5GHz (802.11a/b/g/n) -Bluetooth 4 -Assisted GPS -GLONASS	-Quad-band GSM/GPRS/EDGE -UMTS/HSDPA (Bands I,II,V,VI) -LTE (Bands are regional) -WLAN 2.4GHz and 5GHz (802.11a/b/g/n) -Bluetooth 4 -Assisted GPS -GLONASS

Table 1.1: Comparison of the supported modes/bands for 4 popular smartphones [online source: *www.apple.com/iphone/specs.html* and *http://www.samsung.com/global/galaxys3*].

smartphones from the year 2009 to 2012 are compared. It is seen that the number of supported radio modes have increased from 4 (10 bands) for iPhone 3GS in 2009 to almost 8 (~21 bands) for iPhone 5 in 2012.

A traditional, yet common and straightforward approach to enable multi-mode, multi-band operation is to deploy a separate narrowband receiver or transmitter path for each mode and band. But due to versatility and programmability of some blocks such as down-conversion mixers in the RX path or the baseband and digital blocks, it is possible to share the mixer, the baseband signal conditioning blocks, and the ADC/DAC units [4].

On the other hand, the RF front-ends such as the input or output band selection filters, the duplexers, and the low noise or power amplifiers still lack sufficient flexibility. Since these blocks are the most performance determining blocks along the receiver or transmitter path, they are normally exclusive for each specific band or standard. Table 1.2 summarizes a number of currently popular wireless standards together with their frequency bands, channel spacing, channel access method, modulation scheme, bit-rate, and the required RX sensitivity and signal-to-noise ratio. From this table it is clear that the receiver front-end for each of these standards should meet different requirements in various bands in terms of noise figure, sensitivity etc.

As an example, Figure 1.2 schematically demonstrates the RF blocks that are embedded in the popular iPhone 5 smartphone, incorporating 2G/3G/4G, Bluetooth, WLAN, GPS and FM. It can

System	Bluetooth	WLAN (802.11b)	GPS	FM	2G	3G FDD (WCDMA)[6]	3G TDD (UTRA-TDD)[6]
TX Frequency (MHz)	2402-2480	2412-2484	1575.42	76-108	824-849(GSM850) 880-915(GSM900) 1710-1785(DCS) 1850-1910(PCS)	1920-1980(Band I) 1850-1910(Band II) 824-849(Band V) 880-915(Band VIII)	1900-1920 2010-2025 2300-2400
RX Frequency (MHz)	2402-2480	2412-2484	1575.42	76-108	869-894(GSM850) 925-960(GSM900) 1805-1880(DCS) 1930-1990(PCS)	2110-2170(Band I) 1930-1990(Band II) 869-894(Band V) 925-960(Band VIII)	1900-1920 2010-2025 2300-2400
Channel Spacing	1MHz	25MHz[2]	2.046MHz[1]	100/ 200kHz	200kHz	5MHz	1.6/5/10MHz
Bit-rate	1Mbps	1-11Mbps	1.023Mbps	300kbps[4]	270kbps	3.84Mbps	1.28/3.84 /7.68Mbps
Access	CDMA	CSMA/CA	CDMA	FDMA	TDMA	CDMA	TD-CDMA
Modulation	GFSK	CCK	DSSS/BPSK	FM	GMSK	QPSK	QPSK
RX Sensitivity	-70dBm	-76dBm[3]	-147dBm	0.6μV-1μV	-102dBm	-117dBm	-108dBm/ 1.28MHz
SNR	21dB	10dB	6.5-29dB	55dB[5]	9dB	-18dB/12.2kbps	≈5dB[7]

[1]System Bandwidth
[2]Nonoverlapping channels
[3]According to IEEE 18.4.8.1, to decode 11Mbps data
[4]Up to 300kbps is provided by FM HD radio
[5]For stereo FM
[6]Popular bands
[7]1.28 Mcps TDD option with 384kbps data rate [According to ETSI[2]]

Table 1.2: Specification of popular existing wireless and cellular standards.

be seen that for each WCDMA/GSM/EDGE band an external PA and duplexer/SAW filter is used. Separate SAW filters are also used for GPS, BT/WLAN 2.4 GHz, and WLAN 5 GHz transceivers; hence a total number of 9 external SAW filters for all the transceivers.

To address the requirements for highly mobile devices, manufacturers are in pursuit of small factor solutions with minimal external components to reduce size and allow for flexibility in the function of mobile devices with minimal power consumption. In order to meet the stringent blocking conditions in cellular radios, high performance external SAW filters or duplexers are required. But SAW filters are bulky and expensive; plus, they reduce the receiver flexibility and degrade the RX sensitivity by 2 to 3 dB[3].

[2] http://www.etsi.org/deliver/etsi_ts/125100_125199/125102/11.03.00_60/ts_125102v110300p.pdf
[3] Typical SAW filter loss looked up on the internet.

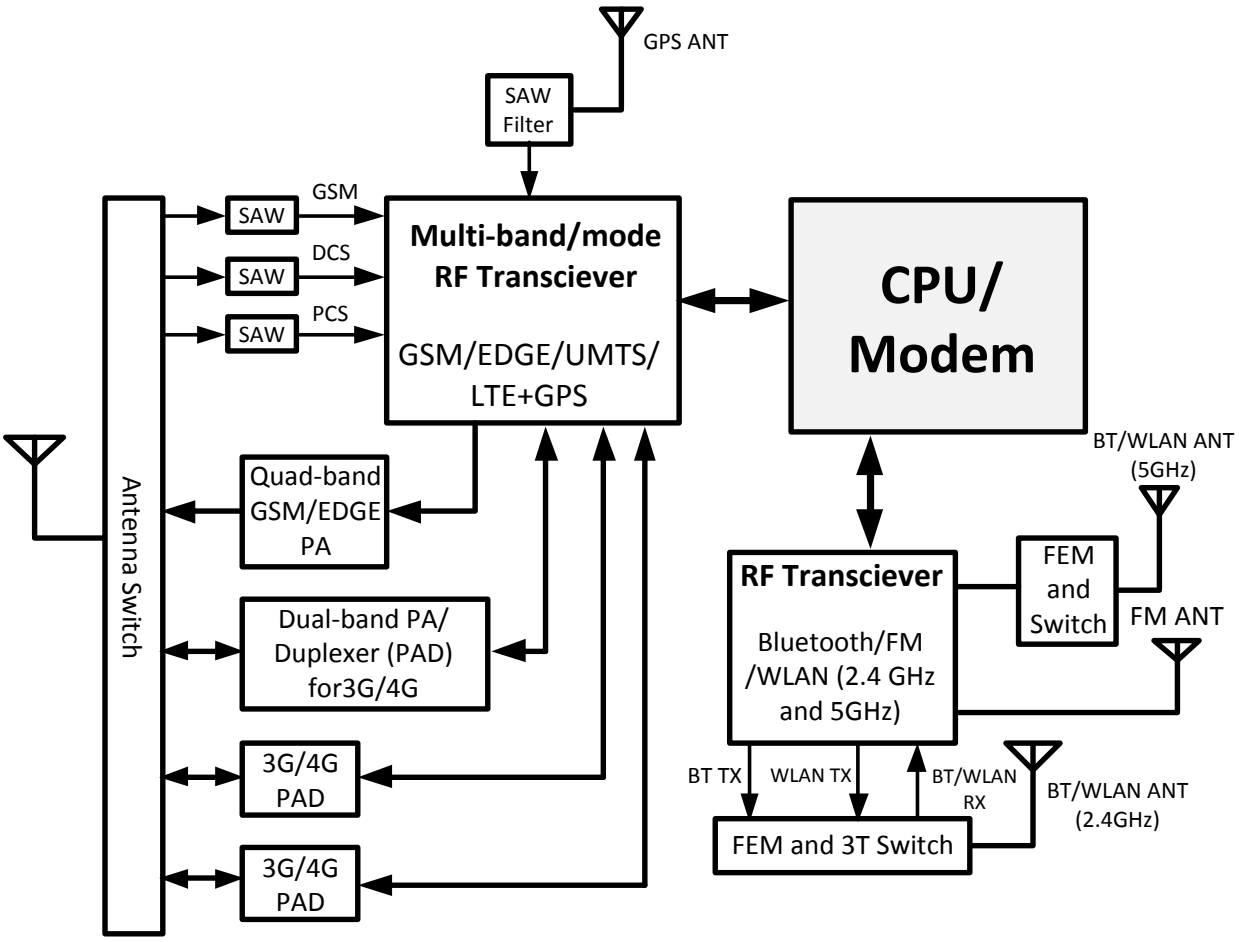


Figure 1.2: A simplified schematic of the newest multi-mode, multi-band iPhone 5 smartphone announced in 2012 [source: *http://www.ifixit.com/Teardown/iPhone+5+Teardown/10525*].

Therefore, "true SAW-less" receivers (by removing the SAW filter at the input of the RX) have been recently introduced by [5] and [6]. SAWless receivers as the ones in [6] or [5], should conform to the blocking profile requirements as specified by 3GPP or other standardization. As an example, a GSM receiver should withstand a 0-dBm CW blocker at 20 MHz away from 850/900 MHz band and at 80 MHz away from PCS/DCS bands [5], and due to the assumption that the blocking conditions are rare a blocker NF up to +15 dB is acceptable.

Additionally, to outlive in the emulous market of mobile devices, evolving consumer products should both incorporate multiple radio interfaces and support features such as high quality camera and color display, MP3 audio playback, digital TV and etc. This calls for large amount of memory, logic and digital signal processing capabilities integrated with analog baseband and RF

circuits. In the spirit of miniaturization and cost minimization, single silicon die integration of RF parts and digital parts becomes very attractive.

Integration has been a clear trend since the advent of silicon technology, and during the past few years RF, analog, digital, and memory integration has shown remarkable reduction of costs and power consumption of the systems by means of single-chip RF SoCs. To further benefit from the integration capabilities, manufacturers can juxtapose multiple RF SoC cores on a single silicon die. Multi-core radio integration enables manufacturers to save space and lessen the equipment bill of materials, thereby cutting the costs, manufacturing thinner equipment, and minimizing power consumption. At the same time, multi-core radio integration enables them to deliver equipment with more connectivity functions.

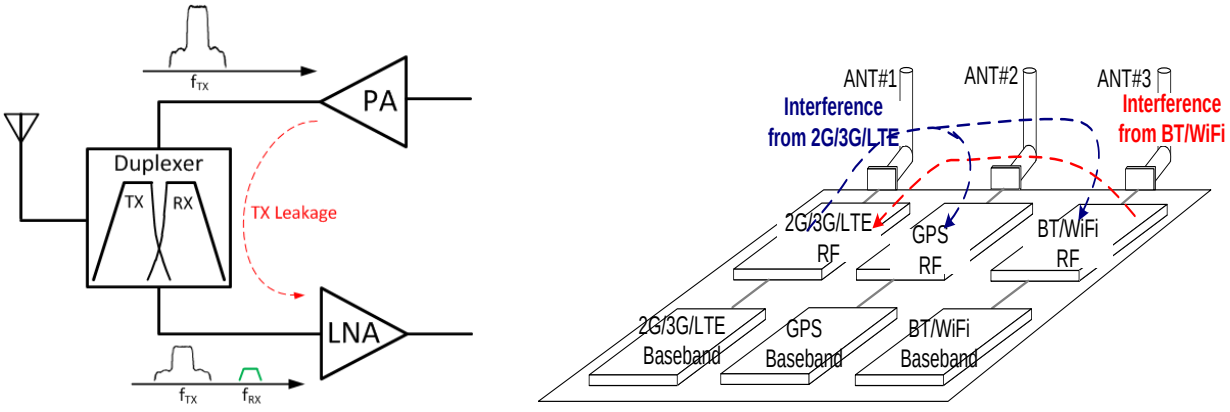
While the SAW-less operation of a receiver is already a challenging task, multi-core radio integration adds to its complexity in two ways: firstly, in many blocking scenarios it is assumed that the interferer rarely occurs [5], so a large margin for degradation in RX performance is allowed (for example in GSM, NF is allowed to increase up to +15 dB under blocking conditions). Although in multi-core radios this assumption can no longer be true since the added value of multi-core radio integration is achieved only when simultaneous operation of multiple radios is allowed. Secondly, due to proximity of antennae in multi-core radios the power of the interferer appearing at the input of the RX can be considerably larger than the values specified by radio standards.

1.2 Electromagnetic Interference in Multi-Core Radio Frequency Integrated Circuits

To enable multiple radios to coexist with in a single piece of silicon while allowing them to operate simultaneously requires knowledge of how the radios impact each other and how their performance is degraded by electromagnetic interference. Although electromagnetic interference is not the only source of interference and microprocessors, switching regulators, LCD drivers, and touch panels etc. all can lead to some sort of interference [7]; nevertheless, only the electromagnetic interference, in particular, is considered here

The simultaneous operation of many radios co-located on a same chip leads to a hostile interference environment as antenna-to-antenna and duplexer isolation has plunged to allow manufacturing of thinner gadgets at lower costs. Furthermore, emerging technologies are going towards smaller duplexers while same-chip integration is bringing the antennae closer, where both trends worsen the isolation.

In general, the primary source of interference is the TX signal of one system (aggressor) impairing the RX performance (remarkably sensitivity) of other system(s) (victim). The aggressor can leak into the RF-front of the victim through the duplexer in FDD systems or through the receiver antenna in two different radio systems, as shown in Figure 1.3.



(a) (b)

Figure 1.3: Two dominant interference sources: (a) Due to limited duplexer isolation. (b) Due to limited antenna-to-antenna isolation [1].

1.3 RX Performance Degradation by Interference

Electromagnetic interference is the main source of performance degradation in a multi-core radio scenario. The aspects of performance degradation are threefold: 1) the leakage of the strong aggressor signal into the RX can degrade its performance due to various nonlinear mechanisms; 2) the RX band aggressor noise leakage can couple into the victim antenna and directly raises the victim RX noise floor; 3) the aggressor leakage into the victim RX RF front-end can undergo reciprocal mixing with the RX LO phase noise and falls into the IF band after the downconversion. These issues are discussed in more details in the following. Depending on the aggressor and victim frequency separation and the type of the blockers (CW or AM), one of the above mechanisms can dominate and degrade the RX sensitivity.

1) Nonlinear mechanisms: critical blocks, such as the LNA or mixer, used at the receivers RF front-end can corrupt the desired RF signal through several nonlinear mechanism. The most important and related mechanisms in the context of multi-radio coexistence for such blocks are: desensitization, cross-modulation, and intermodulation.

Similar to the 1-dB compression point (P_{1dB}), which defines the desired input signal power at which the receiver gain drops by 1 dB, the 1-dB desensitization point (B_{1dB}) is defined as the power of the unwanted input interference (a CW interference) by which the receiver gain drops by 1 dB. The gain reduction is due to the high order (especially 3^{rd} order) nonlinear terms. If the amplifier operates close to its B_{1dB}, 5^{th}, 7^{th} and higher order nonlinear terms should be taken into account to characterize the intermodulation distortion behavior of the circuit. Another implication of RX gain reduction due to a blocker is an increased NF. According to [8], the overall RX NF will increase by 0.2 dB and 0.9 dB for 1-dB and 3-dB gain compression, respectively. To avoid RX desensitization by large blockers, large B_{1dB} is required.

Cross-Modulation occurs when the amplitude variation of one of the signals induces amplitude and phase variations on the other. In this way, the modulation on one channel's carrier might get transferred to another channel's carrier, as shown in Figure 1.4. For a nonlinear RX RF front-end operating well below its B_{1dB} and characterized by only 3^{rd} order nonlinearity term, the cross-modulation product power (P_{XMOD}) at RX band is given by (1.1).

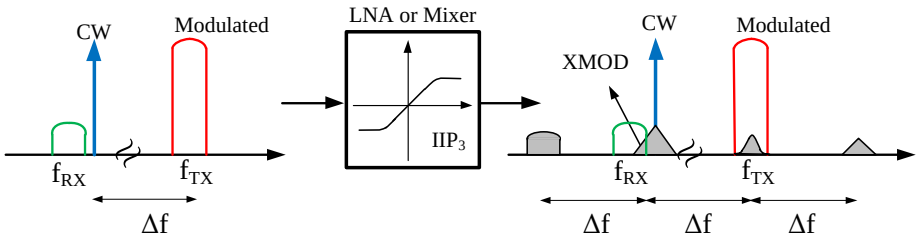


Figure 1.4: Wanted signal corruption due to the cross-modulation of an amplitude-modulated blocker with a CW jammer close to the RX channel

$$P_{XMOD}(dBm) \approx 2P_{MOD} + P_{CWJ} - 2IIP_3 - CF \tag{1.1}$$

$$P_{IMD}(dBm) \approx P_{MOD} + 2P_{CWJ} - 2IIP_3 - CF \tag{1.2}$$

[9]

In (1.1), CF is the correction factor and a function of TX modulation scheme, frequency spacing of CW jammer and RX band, and TX/RX bandwidth. P_{MOD} and P_{CWJ} are the power of the modulated and CW blockers, respectively. As an example, for WCDMA modulated TX CF is approximately equal to +7.4 [9].

A different scenario for the frequency location of the CW and the modulated blocker is shown in Figure 1.5. The modulated interference can be the leakage from an amplitude modulated TX such as WCDMA or Wi-Fi. The intermodulation product of these two blockers can fall into the desired RX band and corrupt the wanted RX signal. The intermodulation product power can be related to the IIP3 of the RX through (1.2).

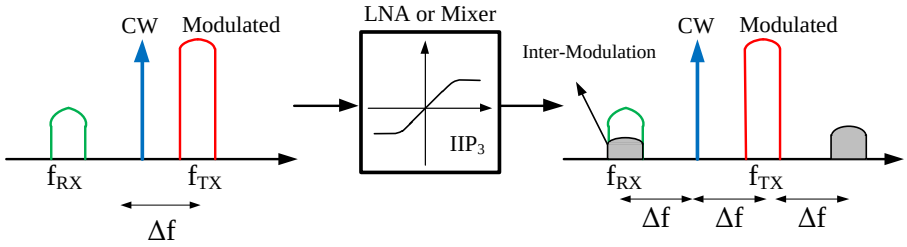


Figure 1.5: Wanted signal corruption due to the intermodulation of an amplitude-modulated blocker (the aggressor TX) with a CW jammer

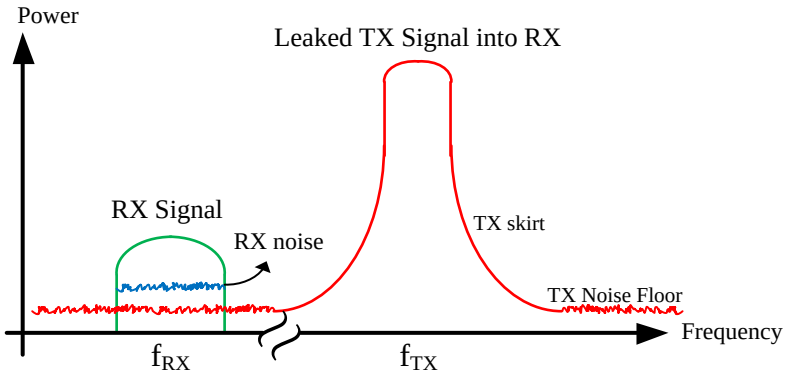


Figure 1.6: RX sensitivity degradation due to the RX band TX noise leakage.

2) Noise leakage: When the TX signal leaks into the RX it can increase to the RX in-band noise, due to the far-out noise of the VCO/DCO and PA used in almost every transmitter. As demonstrated in Figure 1.6, if TX band is spaced closely to the RX band (e.g. 45 MHz for WCDMA band V) the noise skirt of transmitted signal can contribute to the overall noise at the RX band degrading sensitivity.

3) Re-mix from RX LO: As shown in Figure 1.7, reciprocal mixing occurs when strong interfering signals mix with the noise skirts of the RX local oscillator (LO) and get downconverted to the same IF frequency as the desired signal (here in this figure *IF=0*), which consequently can degrade the receiver sensitivity.

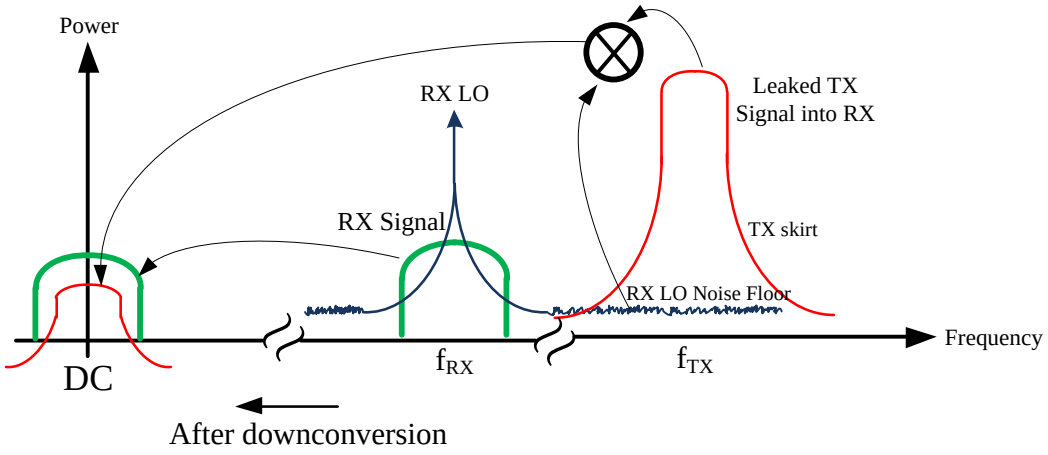


Figure 1.7: RX sensitivity degradation due to RX LO PN re-mix.

1.4 Conclusions of Multi-Radio Coexistence Issues

The following conclusions can be made from the different RX performance degradation mechanism introduced in the previous sections:

1) The TX noise leakage should only be coped with on the TX side. Once TX noise leaks into the RX band at the input of the RX, it is not possible to filter it out. This work focuses on the receiver and this issue is not dealt with here.

2) Reciprocal mixing is directly related to RX LO phase noise at the TX band and the interference leakage power. By filtering or canceling the interference before the mixer the RX sensitivity degradation due to reciprocal mixing can be minimized.

3) To avoid RX desensitization due to the blocker, the RX RF front-end should have a large B_{1dB}. The inter/cross-modulation products are all directly related to the amplitude of the interference and the linearity of the RX RF front-end. Adjacent channels as well as out-of-band blockers may corrupt the receiver performance. As a result, high in-band and out-of-band IIP3 are essential.

1.5 Thesis Organization

The organization of this thesis is as follows. In chapter 2, some techniques, proposed in the literature, that enable the receivers to deal with interference and large blockers are provided. Based on the prior-art, a highly selective, very linear LNTA capable of large-signal handling for current-mode RX front-end is proposed in chapter 3, in addition to the analysis and the simulation results. Chapter 4 deals with the implementation of the proposed LNTA and the measurement results. Finally, the conclusions and the future work are discussed in chapter 5.

Chapter 2

PRIOR ART IN INTERFERENCE ROBUST RECEIVERS

Numerous techniques have been proposed in the literature to enable the receivers to deal with interference and large blockers. Generally, these techniques can be classified into three categories:

1) Interference mitigation
2) Interference cancelation
3) Highly linear receiver RF front-ends

This chapter reviews a number of prior-art related to each of these categories. In the first two techniques, as their names suggest, the interference is reduced by filtering it using on-chip high-Q filtering techniques or cancelling it using an anti-phase replica of the interference, respectively.

In section 2.3, the current-mode receiver topology, as the most suitable candidate for large-signal operation among other receiver architectures, will be discussed. It will be shown that the main linearity bottleneck in the current-mode receiver architecture is the input LNTA. Accordingly, a few state-of-the-art solutions to enhance the LNTA linearity and its large-signal operation will be presented.

2.1 Interference Mitigation Techniques

2.1.1 Blocker Filtering Using Translational Impedance Mixing

A technique that has been used to enhance the compression point of the receiver RF front-end, especially the LNA, is translational impedance mixing, which relies on the input impedance property of passive mixers [10]. According to [6], a low-Q baseband impedance can be frequency-translated to RF using a passive mixer and, therefore, be converted to a high-Q bandpass filter (HQBPF), as demonstrated in Figure 2.1. Although this technique can improve the large-signal linearity performance (such as $P_{1\text{-dB}}$ or $B_{1\text{-dB}}$) of the circuit, it does not affect the small-signal linearity performance (such as IIP3) significantly.

[6] has employed this sort of HQBPFs at the input and the cascode node of a cascoded common-source amplifier, as shown in Figure 2.2, to prevent large voltage swings at these nodes due to large blockers. [6] has shown a simulated -10 dB filtering at 50 MHz frequency offset (or equivalently a BPF with Q of about 150) at the input of the LNA for the structure of Figure 2.2 when the HQBPFs are enabled, which occurs at the presence of large blockers. In the complete receiver implemented by [6], it has been reported that the receiver gain reduces by only 0.8 dB

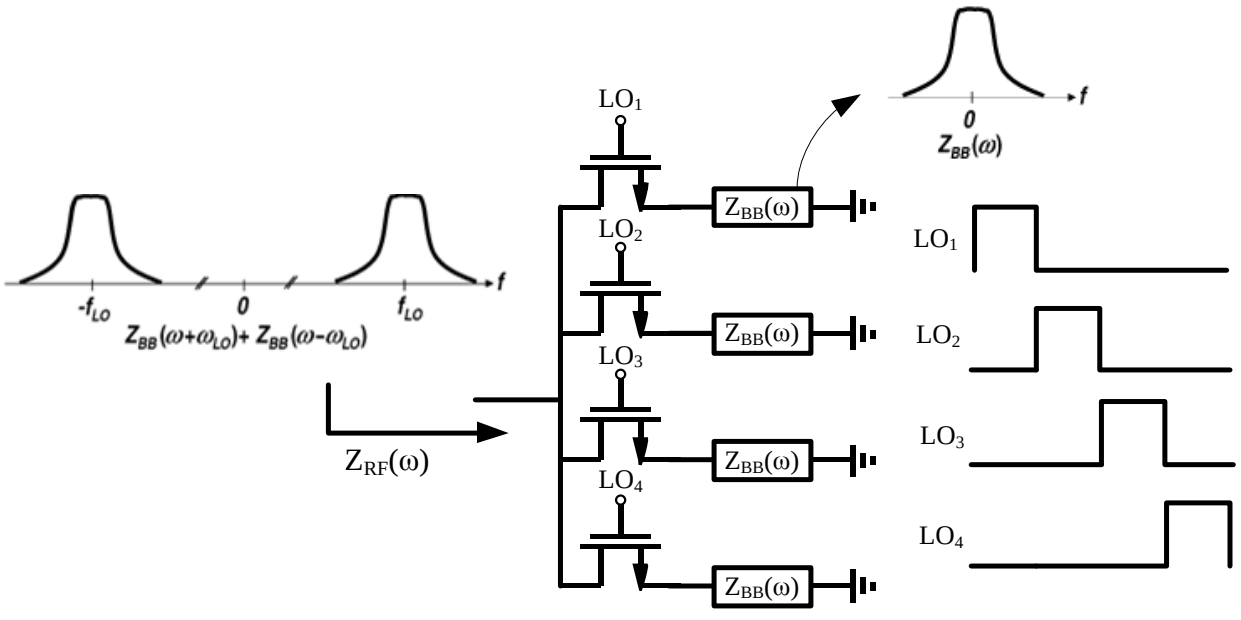


Figure 2.1: Translational impedance mixing property of a current-driven passive mixer [11].

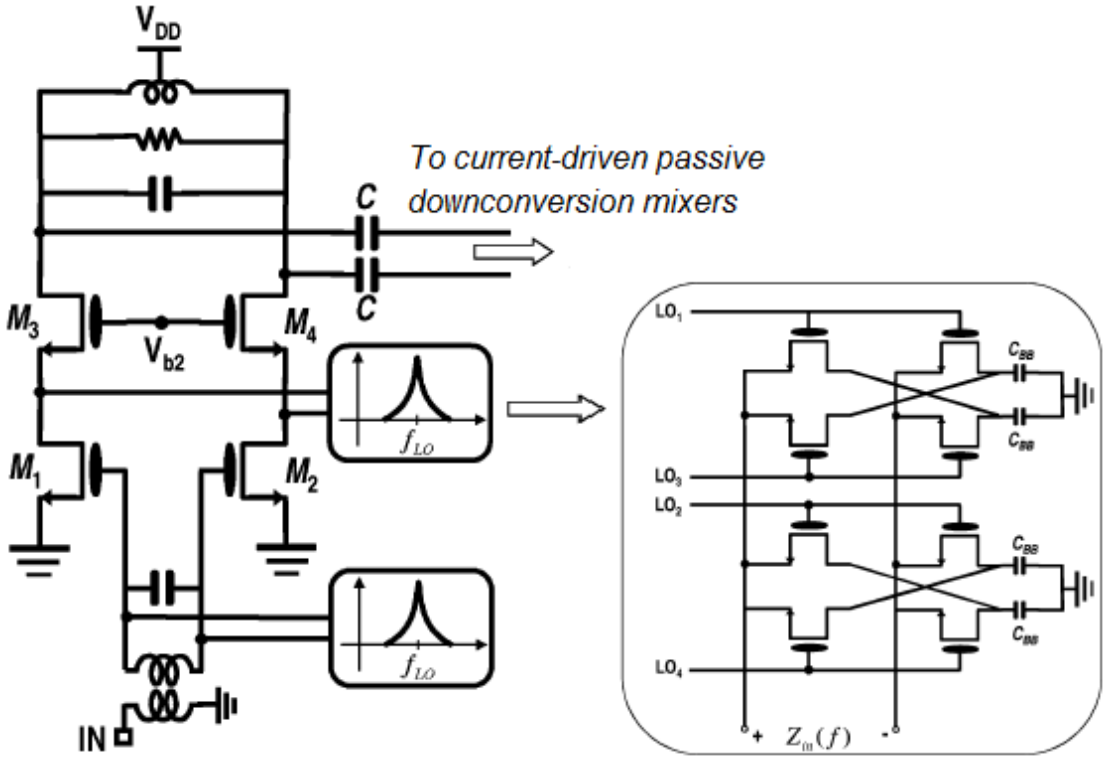


Figure 2.2: The LNA incorporating HQBPFs proposed and implemented by [6].

and NF increases to 10.9 dB at a presence of a 0-dBm blocker at ±80 MHz frequency offset. When the HQBPFs are disabled a NF of 3.1 dB has been reported for the RX, although NF increases to about 8 dB when the HQBPFs are enabled. Since the receiver meets the 3GPP requirements without a SAW filter, [6] has been one the first reported "true SAW-less" quad-band 2.5G receivers in 65-nm CMOS technology.

Another work that has employed the translational impedance mixing property of a passive mixer has been reported in [12], [13]. Using a passive voltage-sampling mixer at the output of the LNA, attenuation of 15 dB at 20 MHz offset frequency is achieved at the output node, hence preventing large voltage swing due to large blockers. The passive mixer is therefore used for both filtering and downconversion purposes. This LNA has been implemented by [13] in 90-nm CMOS technology using 2 V supply voltages and has achieved a wideband 0.4 to 3 GHz frequency operation with less than 3 dB NF. A +1 dBm out-of-band compression point (also

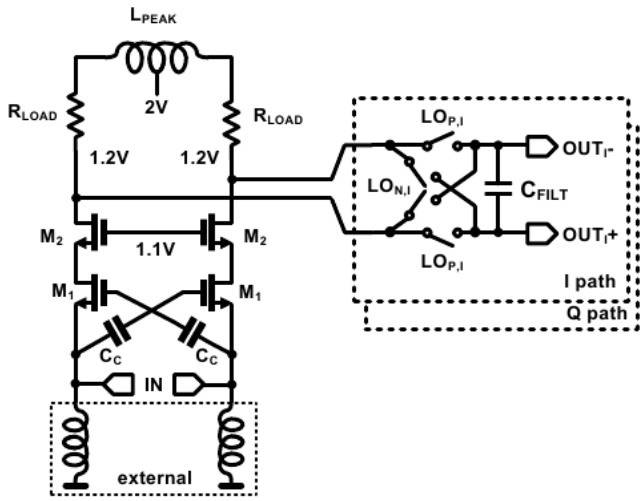


Figure 2.3: A highly-linear LNA with passive voltage-sampling filtering mixer proposed by [13].

known as desensitization point) for a blocker at >60 MHz has been reported. The in-band and out-of-band IIP3 for this LNA has measured +11 dBm and +18 dBm, respectively.

2.1.2 RF Sampling and Discrete-Time Signal Processing

Recent works such as [15], [16], and [14], have shown discrete-time receiver architectures, which the RF signal is sampled at early stages with charge-domain sampler and filtered using switched-capacitor (SC) filtering techniques. The implicit anti-aliasing filter prior to sampling and subsequent FIR and IIR filters can strongly attenuate alias and adjacent channels and allow sampling of the signal at lower rate at the ADC stage. This technique is very beneficial for software-defined radio (SDR) applications, where flexible receiver topologies are required.

As an example, in the flexible DT receiver architecture proposed by [14] and shown in Figure

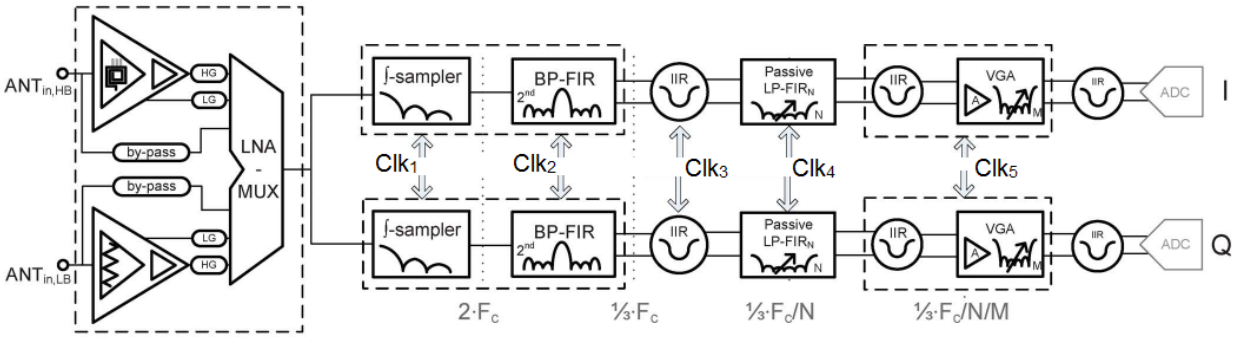


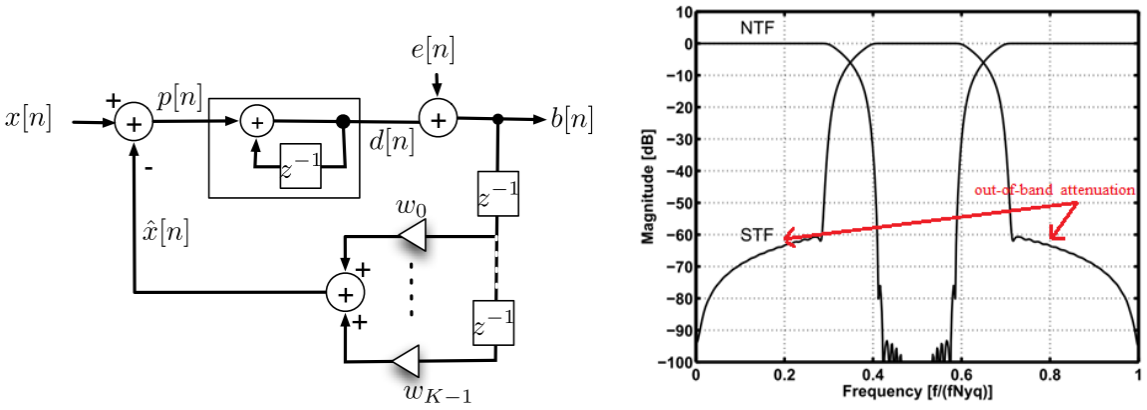
Figure 2.4: Flexible DT receiver architecture proposed by [14].

2.4, the input is sampled at the Nyquist frequency and band-pass filtered via a $sinc^2$ FIR filter, which also downconverts the signal by means of subsampling. The filter provides strong OB attenuation at RF, as well as anti-alias filtering for sample rate decimation. A multi-band LNA is used at the input of RX before converting the RF signal to current via a transconductor amplifier, which is not implicitly shown in Figure 2.4. Basically, the total RX chain can provide flexible and strong filtering, and the linearity performance of the receiver is enhanced via immediate strong filtering of interference at the output of TA. However, the input LNA can still saturate and desensitize the receiver at the existence of strong out-of-band blockers. [14] has reported an in-band and out-of-band IIP3 of +2.5 dBm and -13 dBm, respectively, and 5.3 dB NF for GSM band.

2.2 Interference Cancellation Techniques

2.2.1 ΔΣ Receiver with RF Feedback for Adaptive Interference Cancellation

In a $\Delta\sum$ modulator with feedback, as shown in Figure 2.5 (a), the feedback weights, denoted as **w**, can be selected in such a way that maximum cancellation of unwanted interference signal (at out-of-band frequencies) is achieved before the quantizer, which is the critical part in terms of the dynamic range. To simply demonstrate the working principle of this method, constant **w** coefficients can be assumed. By deriving the signal transfer function (STF) and noise transfer function (NTF) of a multi-feedback $\Delta\sum$ modulator, it can be seen that, by adjusting the coefficients, band-pass and band-stop transfer functions for the signal and noise, respectively,



(a) (b)

Figure 2.5: (a) A Multiple feedback $\Delta\sum$ ADC [17]. (b) Signal and noise transfer functions for the band-pass $\Delta\sum$ modulator proposed in [18] with constant feedback weights.

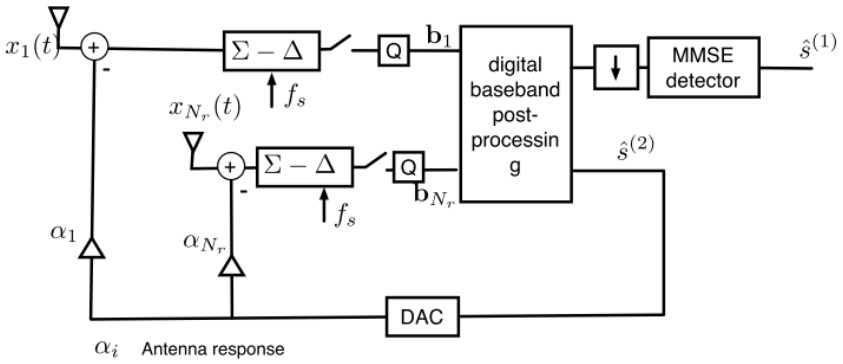


Figure 2.6: $\Delta\sum$ receiver with RF feedback for adaptive interference cancellation [17].

can be implemented. For instance, signal transfer function can have a flat response at the pass-band and attenuation for out-of-band signals, and thus, an implicit filtering function. If used at the front-end of a receiver, the out-of-band blockers can no longer decrease the dynamic range of the receiver. An example the transfer functions of a band-pass $\Delta\sum$ modulator with multiple feedbacks that demonstrates this powerful property is demonstrated in Figure 2.5 (b).

The signal and noise transfer function shaping approach can now be extended further by adoptively computing feedback weights [17]. The feedback coefficients can be predictively estimated by DSP based on the interference data. [17] has shown a joint RF-Baseband interference cancellation RX topology, schematically demonstrated in Figure 2.6, to cancel interference between different users in a MIMO radio system. By estimating the interfering user and providing feedback to the input of ADC, with proper coefficients computed by DSP, interference cancellation and quantization of the RF signal are combined into one operation.

2.2.2 Active Feedforward Cancellation

Recently, [19] has presented an active feed-forward cancellation topology to cancel out the out-of-band interference without using SAW filters. As shown in Figure 2.7, the down-conversion mixer in the auxiliary path down-converts both the desired signal and the interference. The desired signal is filtered out using a high-pass filter, and the unfiltered interference is up-converted and subtracted from the output of the LNA. By using this topology, a narrowband bandpass (with large Q) response is basically forged at the RF front-end of the receiver. In [19],

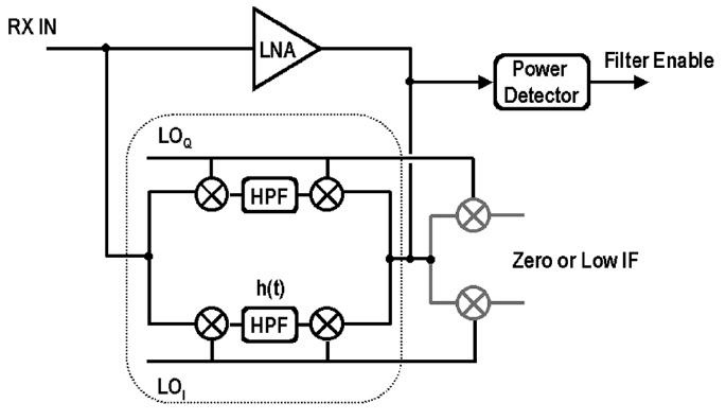


Figure 2.7: Active feed-forward cancellation topology proposed by [19].

the bandwidth of the LNA narrows down from 220 MHz to 4.5 MHz with 21 dB stop-band attenuation.

While this topology can potentially improve the linearity requirement of the LNA output and the following downconversion mixer, it does not relax the linearity requirement at the input of the LNA (the input devices can be driven into compression by the blockers). This technique also suffers from significant increase in noise and power consumption, and its blocker filtering effect depends on the matching between the main and the auxiliary path.

2.2.3 Direct ΔΣ Receiver

[20] has proposed an interesting approach and very similar to the concept presented in [18] or [17], that use a $\Delta\sum$ topology with weighted feedbacks. The receiver front-end in [20] is based on a direct $\Delta\sum$ feedback up-converted to RF and the N-path filtering technique, as schematically shown in Figure 2.8. It is seen that the mixer and ADC are combined within this architecture, and the feedback from the output of $\Delta\sum$ is up-converted to RF and subtracted from the output of first stage LNA, resulting in high-linearity performance. The N-path G_m-C filter embedded within this architecture can provide narrow-band RF filtering response around LO frequency and sufficient selectivity, and the outermost $\Delta\sum$ feedback loop enables noise shaping. Merging RF and $\Delta\sum$ ADC provides inherently high-linearity and sharp band filtering. The channel filtering can be performed in the digital domain.

[20] has reported an RX IIP3 of +4 dBm and -12 dBm at offset frequency of 95 MHz and 10 MHz, respectively. Although for a -20 dBm blocker at an offset frequency of 80 MHz, NF

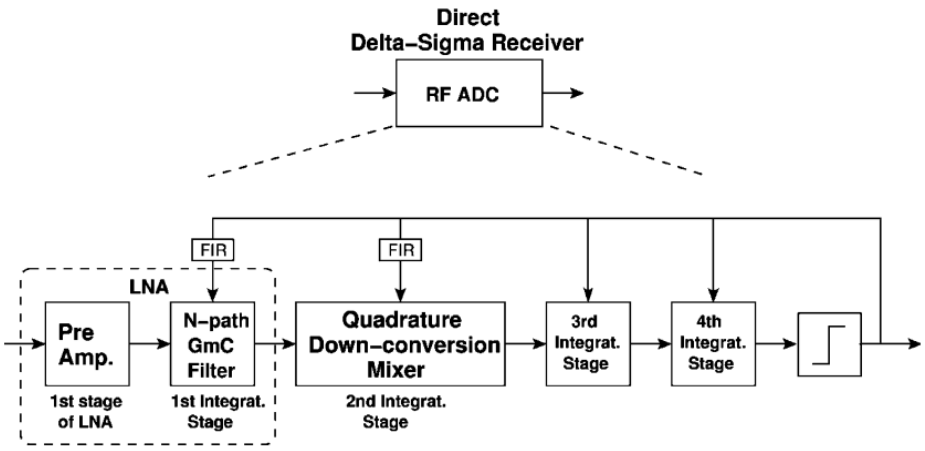


Figure 2.8: A direct $\Delta\sum$ receiver topology with weighted RF feedback [20].

increases to approximately 13 dB, suggesting that this architecture is useless for large blockers at the input. While this architecture significantly enhances linearity and can be efficient and flexible for interference cancellation via optimum adjustment of feedback weights, it still cannot tolerate large blockers, and the NF without any blocker is poor (6.2 dB). The main reason behind this is the injected noise from the feedback loop, which is the main bottleneck of noise performance in this topology. An FIR filter is used to filter out injected noise originating from the feedback loop as much as possible. However, the in-band signals should not be filtered; otherwise the feedback loop fails to operate. Thus, the in-band noise is also always injected to the input and its filtering is not possible. Nevertheless, if a low-noise topology for injecting the feedback signal to the input can be devised, this approach will be promising for adaptive interference cancellation.

2.2.4 Echo Cancellation

In echo cancellation, the interfering transmitter is sampled and used to generate the anti-phase replica of the blocker signal, which is coupled to the LNA input to cancel the blocker. This approach has been employed by the Quellan noise canceller [21], which is schematically shown in Figure 2.9. In Quellan noise canceller, a replica of the aggressor signal (in their case Bluetooth) has been derived from the TX to generate the anti-phase signal matched to unwanted narrowband noise. A tunable bandpass filter has been used to filter out the far-out noise of the anti-phase replica generator that falls into the RX band (in their case 802.11b WLAN receiver), so as not to impair the RX sensitivity. The replicated interference is then subtracted from RX input by coupling the energy of anti-phase undesired signal replica through a capacitor. A 15-dB

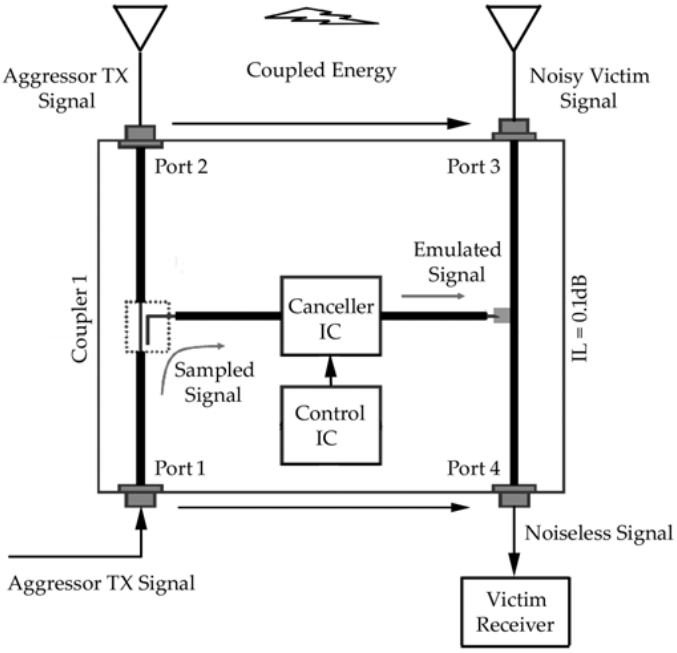


Figure 2.9: Quellan noise canceller architecture [21], [22].

attenuation of the Bluetooth aggressor has been reported in [21]. The power of the injected noise to the RX band is less than -173 dBm/Hz, which leads to almost 2.7 dB WLAN RX sensitivity degradation. The main drawback of this technique is high power dissipation (20 mW) for the canceller unit and utilization of an extra chip to cancel interference between just two radios. Since the proposed architecture is analog intensive, it is challenging to integrate it with existing receivers and technologies.

2.3 Highly Linear RF Front-Ends

2.3.1 Current-Mode Receiver Architectures

The operation region of a MOS device is dictated by its terminal voltages, rather than its current. Therefore, for large gate-source or source-drain voltage swings, the devices can easily enter into the triode region and lead to small-signal gain reduction and linearity issues. These problems are even more pronounced in deep-submicrometer MOSFETs due to the supply voltage reduction and high-field mobility effects [23]. To prevent these issues when large-signal handling is necessary, operation of a receiver in the current domain is preferred [24], which is the concept behind the current-mode receiver architectures.

In a current-mode receiver topology, shown in Figure 2.10, a low-noise transconductance amplifier (LNTA) is utilized to convert the RF input voltage to RF current. Subsequently, a passive current mixer performs the downconversion of this RF current to IF current, which flows into a transimpedance amplifier (TIA) and converted back to voltage at IF. Since the TIA usually provides sufficient low-pass filtering at IF, more stages with voltage can follow the TIA to achieve several orders of magnitude voltage gain before the ADC, with insignificant impact on linearity and noise [25]. Due to the relatively low in-band impedance of the TIA, which can be upconverted to the RF side of the passive mixer [5], the LNTA current flows into mixer and down-converted to IF, leading to small voltage swing at the output of the LNTA. Therefore, the linearity performance of the LNTA and the overall RX can be improved.

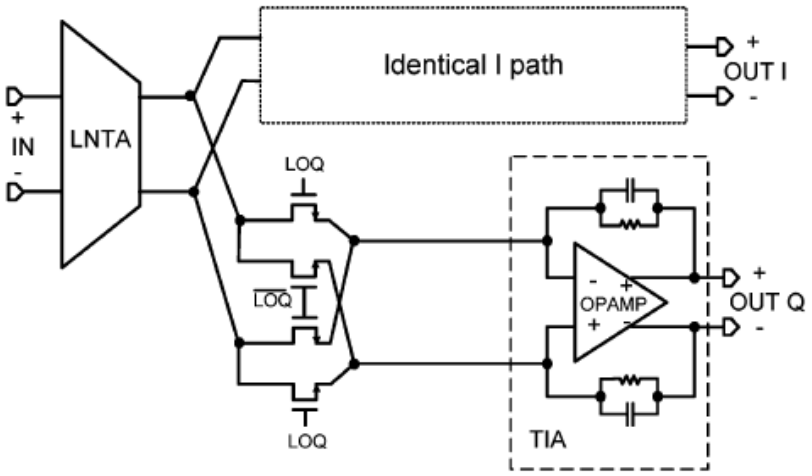


Figure 2.10: Current-mode receiver architecture [5].

To suppress the noise of the stages following the LNTA (namely, the passive current mixer and the TIA), it has been shown that the LNTA transconductance should be large [5]. A large transconductance implies a large current swing through the LNTA. The problems arising from this issue are threefold:

1) Although the impedance at the RF side of the passive mixer is relatively low, the blocker-induced large current swing through the LNTA can still lead to significant voltage swing at the output of the LNTA. As an example, for a 0-dBm blocker with a specified full-circuit LNTA g_m of 120 mS, the blocker current swing flowing into the downconversion mixer is approximately equal to 38 mA peak-to-peak. Assuming a 10 Ω load impedance at output of the LNTA, this leads to 380 mV peak-to-peak voltage swing.

2) As discussed in section 1.3, the sensitivity degradation due to the LO phase noise reciprocal mixing (PN re-mix) is proportional to the magnitude of the blocker. For SAWless applications, since there is no sufficient filtering prior to the passive current mixer, the large blocker current flowing through the mixer can lead to significant sensitivity degradation due to the LO PN re-mix.

3) While the linearity bottlenecks can be relaxed in other parts of the RX due to the current-mode operation, the LNTA still needs to handle large blockers at its input with affordable power consumption. This is very challenging if a class-A biasing scheme is used for the LNTA. For the abovementioned example (0-dBm blocker, $g_m = 120mS$), to accommodate the blocker current swing, the current consumption should be more than 20 mA.

One way to deal with these issues is to mitigate the blocker before it can produce large voltage swing, hence large current swing, at the input of the LNTA. The on-chip high-Q bandpass filters by using passive mixers [6], which were discussed in section 2.1.1, basically attempts to accomplish the interference mitigation before the LNTA.

From the above discussions, it can be concluded that the main linearity bottleneck for the current-mode receiver architecture is the LNTA. Recently, a few works have addressed this issue, some of which will be discussed in the following section.

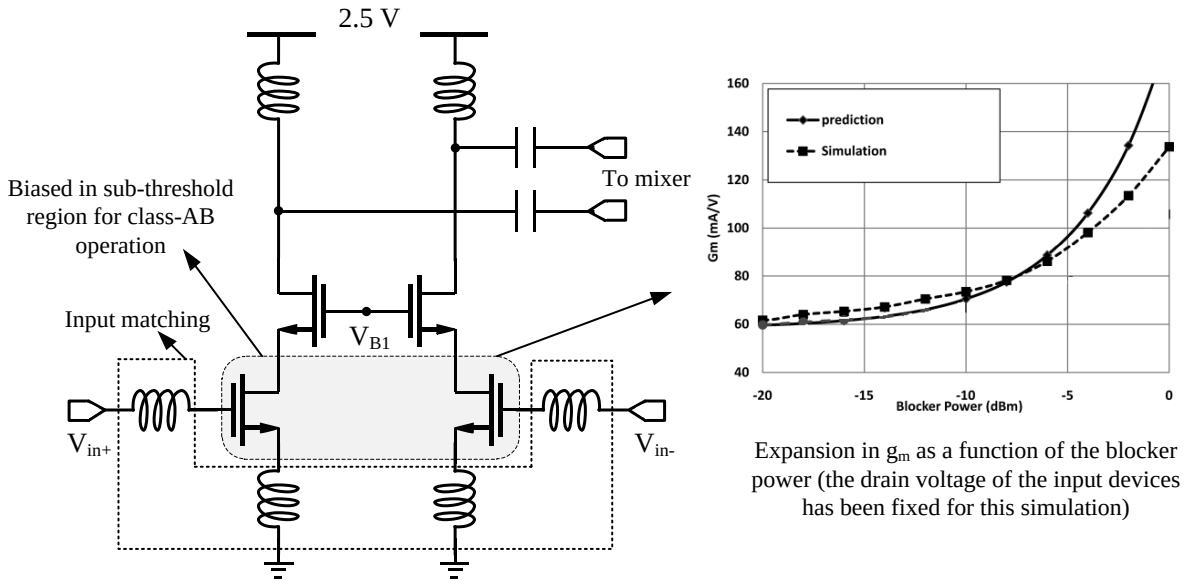
2.3.2 Large-Signal Handling Low Noise Transconductance Amplifiers

For a typical receiver, the key task of an LN(T)A is to provide low nose with large small-signal gain to suppress the noise form the subsequent stages. In a SAW-filter-based receiver, the out-of-band large blockers are usually sufficiently mitigated. Therefore, it is assumed that the LNTA operates well below its compression point, which for a typical narrowband design is around -15 dBm [5].

The RX linearity performance metric (IIP3) is achieved by extrapolation from the small-blocker slope-of-3 region of the IMD curve [24]. So the IIP3, that is commonly used to assess the magnitude of intermodulation distortion, is not actually measured at the power level even close to the actual blockers. As the input power increases, higher order nonlinearity terms start to dominate and IIP3 cannot be used to predict IMD products.

Common linearization techniques rely on the fact that LNTA operates well below its compression point and merely try to improve the "small-signal linearity" performance of the LNTA (IIP3). For instance, the multiple gated transistor linearization technique [26] and/or the third-order distortion cancellation technique by combining a common-gate and common-source amplifiers [27] work well only for a small voltage range, and are not generally suitable for large-signal applications. As a result, the proposed LNA in [27] has achieved +16 dBm IIP3 only for blockers as large as -20 dBm. As the blocker power exceeds this number, the odd-order IMD products start to increase, exacerbating the distortion.

To improve the compression point of the amplifier while avoiding the universal power-linearity tradeoffs that exist for common class-A amplifiers, a class-AB biasing scheme can be employed. In the class-AB common-source LNTA proposed by [5], presented in Figure 2.11, it has been shown that by biasing the input devices in the sub-threshold region, due to the exponential relationship between the drain current and gate-source voltage, similar to that of a bipolar transistor, g_m of the input device expands as a function of the input power. This expansion can compensate for the compressive behavior in other parts of the circuit, such as the cascode device. This leads to a flat response in the g_m of the LNTA as a function of the blocker power, which translates to a large compression point. A measured desensitization point of +1 dBm and an in-band IIP3 of 0 dBm has been reported by [5].



Expansion in g_m as a function of the blocker power (the drain voltage of the input devices has been fixed for this simulation)

Figure 2.11: The class-AB self-bias LNTA proposed by [5] and the desirable gain expansion behavior due to class-AB input devices.

Based on the improved large-signal performance of class-AB amplifiers, [24] has proposed a push/pull class-AB common-gate amplifier, shown in Fig X. The expansion in the g_m of the input devices, which is caused by the class-AB operation of the transistors, is compensated with compressive effects such as the mobility degradation and transition into the triode region. As a result, the output-current input-voltage characteristic of the LNTA remains relatively flat for even large input swings. A very large simulated +22 dBm 1-dB desensitization point has been reported in [24] for an ideal load impedance of 0 Ω.

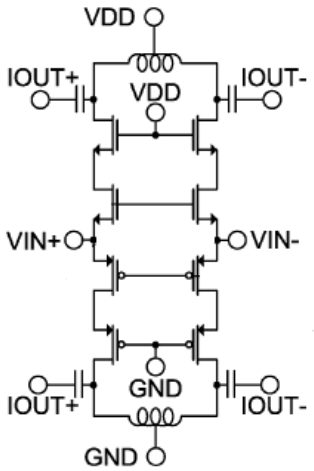


Figure 2.12: Simplified schematic of the push/pull class-AB common-gate LNTA proposed by [24].

Chapter 3

AN INTERFERENCE ROBUST, HIGHLY SELECTIVE LOW NOISE TRANSCONDUCTANCE AMPLIFIER

The prominent challenge in multi-radio chips is blocker interference. In order to meet the stringent blocking conditions in cellular radios, external SAW filters or high performance duplexers are required. However, SAW filters increase cost, reduce the receiver flexibility, and degrade the RX sensitivity by 1.5 dB [6] to 3 dB. Consequently, "true SAW-less" receivers (by removing the SAW filter at the input of the RX) have been recently introduced by [5] and [6].

Currently, it is a popular practice for the manufacturers to cover multiple bands and standards, on the receiver side, by deploying multiple LNAs or mixers. Although, to achieve the ultimate flexible and multi-core radio operation, a single wide-band LNA is desirable to be employed for all the intended frequency bands

Therefore, to enable the true multi-radio operation, for the future RF transceivers, with affordable power consumption and complexity, wide-band LN(T)As with large-signal handling capabilities seem to be essential. Not only for multi-band multi-radio applications, but also for

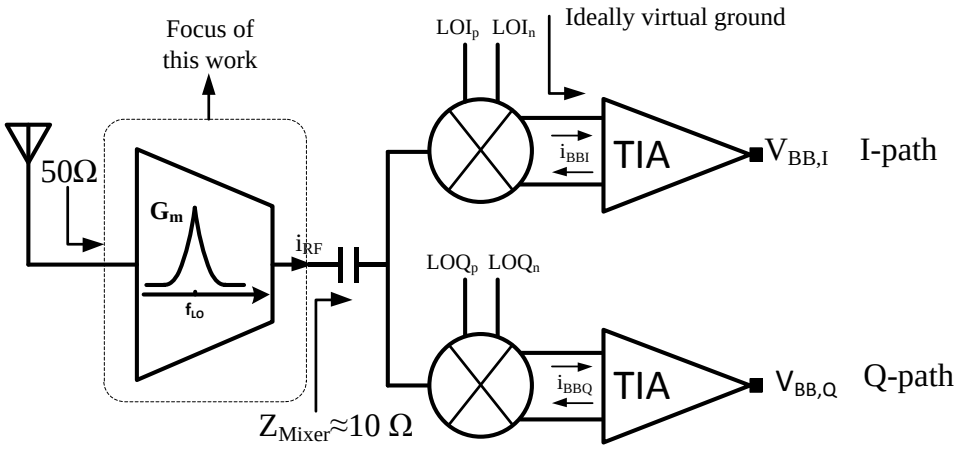


Figure 3.1: Current-mode receiver architecture used as the context for the design of the proposed LNTA.

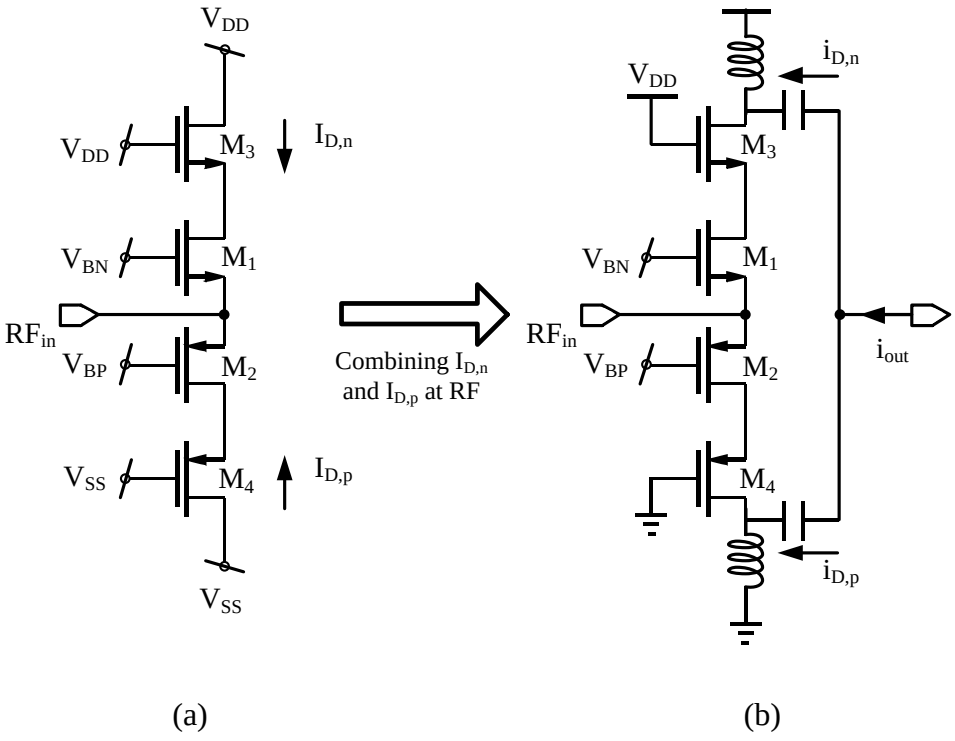
applications such as TV cable modems, software defined radios, and ultra-wideband applications, wideband and highly linear LN(T)As are of great interest [28].

It has been indicated in several works ([5], [6], [24]) that direct conversion receivers with passive current mixers, as shown in Figure 3.1, usually have superior performance in tolerating large blockers. This property stems from the fact that the load impedance of the low noise transconductance amplifier (LNTA), which is the impedance at the RF side of the current passive mixer, is usually designed to be relatively small. Ideally, a virtual ground should appear at the output of the LNTA to suppress voltage swing at this node, across the mixer switches, and prior to the baseband filters. Therefore, this architecture reduces the linearity bottlenecks at the LNTA output and other parts of the RX. However, the LNTA input is still required to able to tolerate the large blockers at its input without desensitization and significant NF degradation.

In this work, we propose an LNTA that is highly robust against interference. The proposed LNTA is assumed to be used is the context of current-mode RX architectures, as shown in Figure 3.1. The LNTA load impedance is determined by the input impedance of the passive mixer with the TIA load [29]. It will be demonstrated further in this chapter that for the best linearity performance, the load impedance of the LNTA should be made as small as possible. Consequently, the RX RF front-end is guaranteed to maintain its current-mode operation, which is very beneficial to its large-signal handling capability. According to the literature [30], the load impedance of the mixer is estimated to be as small as 10 Ω for the analyses and discussions of this chapter.

3.1 Achieving High Selectivity and Linearity by Combining Push/Pull Class-AB CG Stage with On-chip HQBPFs

The core part of the LNTA proposed in this work is a push/pull class-AB common-gate (CG) stage that is adopted from [24] and shown in Figure 3.2 (a). A feature that renders the cascoded CG amplifier of Figure 3.2 (a) suitable for large-signal operation is that the drain voltage tracks the input voltage (neglecting the body effect). Assume that the cascode devices have the same size and biasing conditions as the input transistors. By changing the input voltage by the amount of ΔV, the source voltage of the cascode device changes approximately by ΔV, since the same current flows into the cascode transistor. Hence, the drain-source voltage of the input transistors remains roughly constant, which improves their linearity [31]. In addition, since V_{DS} remains constant while V_{GS} increases, a class-AB operation can also be expected from the cascoded structure of Figure 3.2 (a). The class-AB operation is beneficial due to the fact that it relaxes the universal trade-off between power consumption and large dynamic range (or linearity) that exists for typical class-A amplifiers [5][24] .



(a) (b)

Figure 3.2: Stacked push/pull class-AB CG stage used by [24] to enable "rail-to-rail" input swing. (b) Topology proposed by [24] to combine the output currents at RF.

On the contrary to class-A amplifiers, where current in the transistors flow during the entire period of a sinusoidal input, in class-B or class-AB structures, the current flows in each transistors for less than the entire period of a sinusoidal input. Depending on their bias point, push/pull amplifiers can operate as either class-B or class-AB amplifiers. Although class-B amplifiers have more power consumption efficiency, they lead to significant amount of distortion due to their dead-zone. Therefore, in order to improve the linearity of the amplifier, class-AB operation is more desirable, since the dead-zone is eliminated, and the amplifier can provide amplification for even small signals. Figure 3.3 demonstrates an example waveform of the large-signal current flows for the structure of Figure 3.2 (a), for a +5 dBm input signal. The push/pull operation is evident from these waveforms. In addition, the DC current of the amplifier, which is 1.4 mA for no input signal, increases to 4 mA, verifying the class-AB operation.

Based on the abovementioned advantages of the push/pull class-AB CG stage, [24] has proposed a structure similar to the one shown in Figure 3.2 (b), where the RF currents flowing through the top and bottom branch are summed by hardwiring the output nodes at RF. [24] has shown that this toplogy ensures a relatively constant g_m over large input swings, which means large

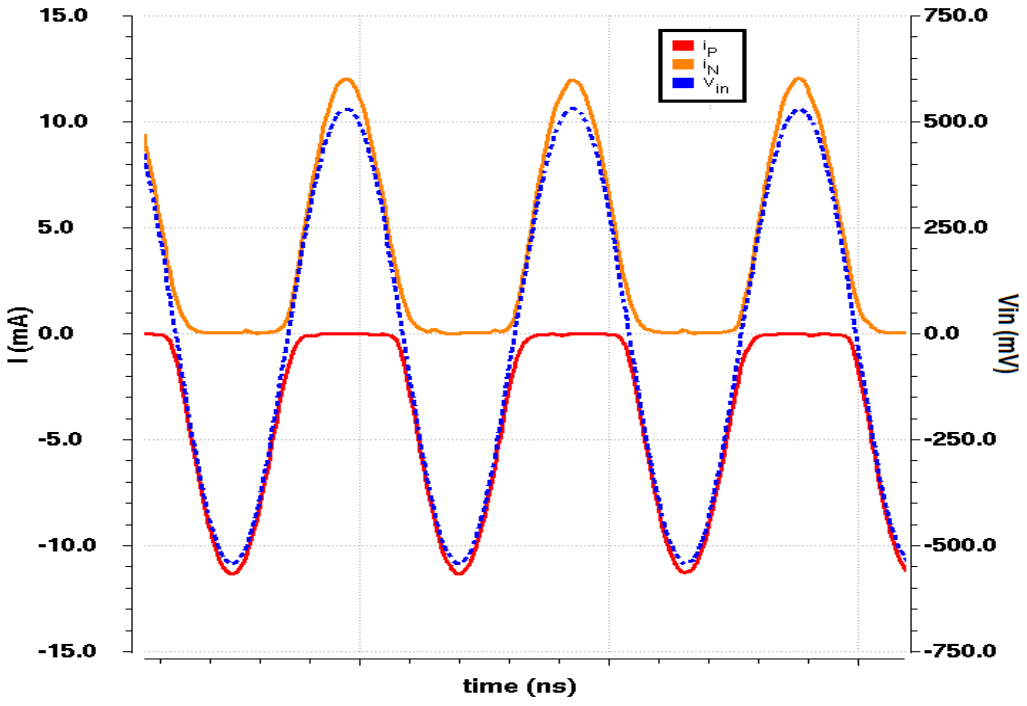


Figure 3.3: Example waveform of large-signal current flows for the structure of Figure 3.2 (a), demonstrating its push/pull class-AB operation.

compression point and good linearity performance. A 1-dB desensitization point of +22 dBm has been reported in [24] for the push/pull class-AB CG stage.

The input impedance of the CG LNTA is controlled via the transconductance of its input transistors, neglecting the drain-source impedance. Therefore, the g_m of this amplifier will be fixed and approximately equal to 20 mS for a 50-Ω source impedance match. For such small value of g_m, the stages following the LNTA, namely, the downconversion mixer and the baseband stages following it, will substantially impact the overall noise performance of the receiver. Therefore, in the receiver proposed in [32], which employs the push/pull CG amplifier of [24], a large NF of 10.7 dB has been reported.

One way to improve the noise performance of the push/pull CG stage is through the modification shown in Figure 3.4. It can be shown that the effective transconductance of the LNTA increases by a factor proportional to Z_L and the g_m of the second stage (consisting of M_5 and M_6). With a large g_m, the noise contribution of the stages following the LNTA can be suppressed [5]. A

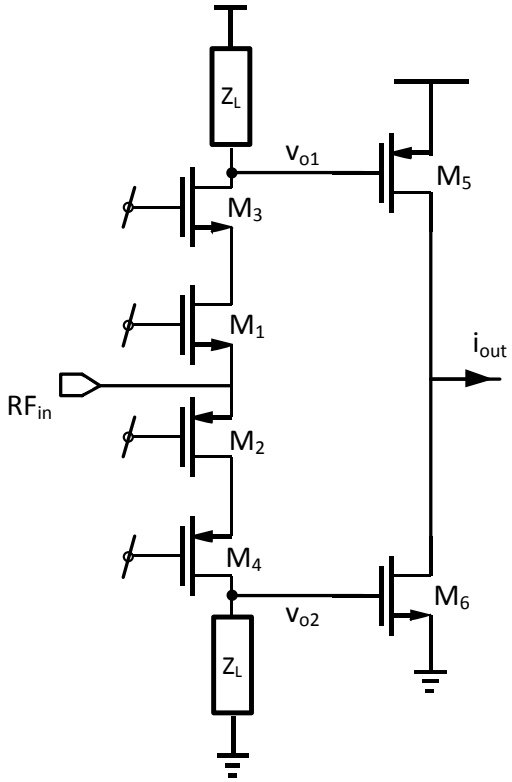


Figure 3.4: Modification in the push/pull common-gate LNTA to improve its noise performance while maintaining the push/pull structure.

similar concept has been shown in [33], in which the cascode devices are omitted and Z_L is simply implemented via a resistor. v_{o1} and v_{o2} are then combined by hard-wiring them at RF. This way the LNTA will not operate as a true push/pull amplifier and losses its advantage for large-signal operation. [33] has reported a measured 1-dB compression point of -12 dBm.

It should be noted here that the successful large-signal operation of the push/pull CG topology of Figure 3.2 (b) depends on its load impedance, which ideally should be zero (or a virtual ground). This has been accomplished in [24] by employing a passive current mixer right after the LNTA.

The effect of the CG stage load impedance on its large-signal performance can be investigated by simply replacing Z_L in Figure 3.4 with resistors and ignoring the second stage. Preliminary compression simulations were performed using Spectre RF PSS analysis, with the bias current equal to 1.4 mA and the input matched to 50 Ω. Moreover, the DC voltage of the cascode transistors was kept constant and equal to 0 V and 1.5 V for PMOS and NMOS cascode transistors, respectively. A CW signal was then applied to the input of the amplifier while sweeping its power and the output currents were monitored. Figure 3.5 shows the normalized transconductance as a function of input power for various load impedances. It can be seen that

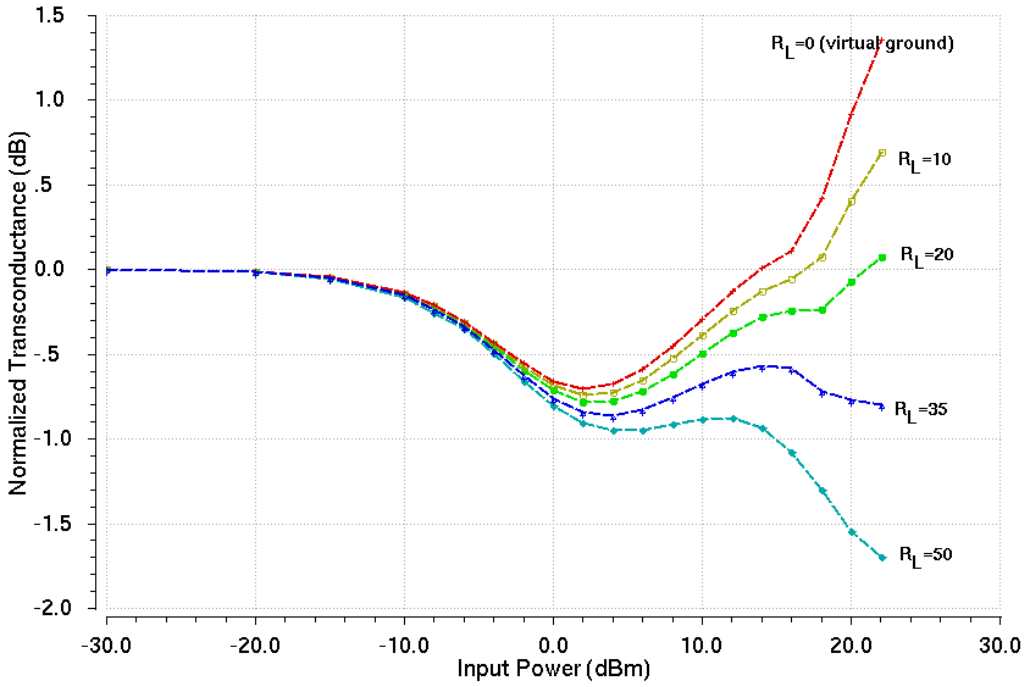


Figure 3.5: Normalized transconductance of the push/pull CG stage with pure resistive loads versus input power for various values of the load impedance.

the amplifier shows a perfect class-AB behavior for R_L= 0 Ω. As the load impedance increases, the gain starts to compress and for R_L > 35 Ω, the gain expansion, thus the class-AB behavior completely disappears.

From the above discussions and simulations, it can be concluded that to achieve good noise performance Z_L needs to be large. However, large-signal performance strongly degrades for R_L > 35 Ω. Therefore, Z_L needs to be a frequency-selective load impedance with a large Q-factor, to provide large impedance for in-band signals and low impedance for out-of-band blockers at an offset frequency of about 100 MHz. This can be achieved by the circuit proposed in Figure 3.6. By using the impedance transformation of a passive mixer (section 2.1.1) an on-chip high-Q bandpass filter (HQBPF) can be realized [6]. By employing the HQBPF as a load impedance, similar to the proposed LNTA of Figure 3.6, we are able to benefit from the large-signal handling capability of a push/pull common-gate stage, while improving its noise performance.

Incorporation of the on-chip high-Q bandpass filters at the sensitive nodes of an LNTA to achieve better large-signal performance has been first reported in [6]. The high-Q band-pass

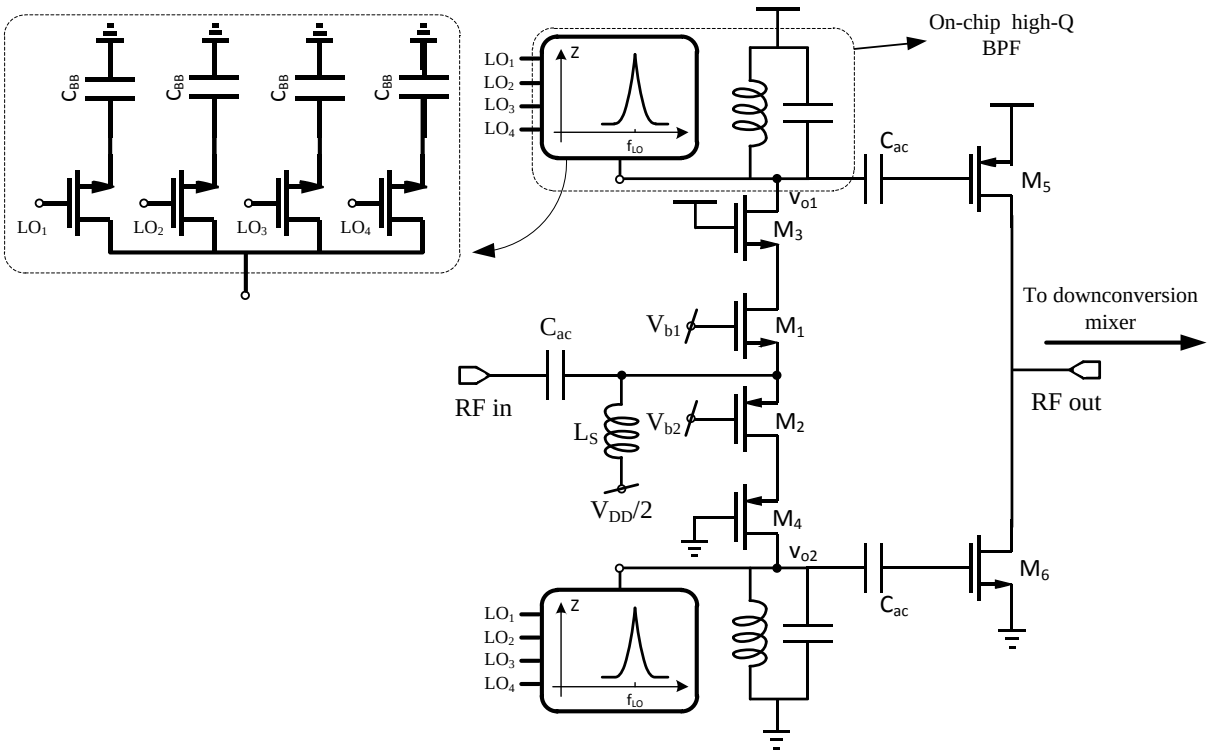


Figure 3.6: The simplified schematic of the proposed LNTA before noise cancellation.

filters (HQBPFs) were inserted at the input of the LNTA and the cascode node of a cascoded common-source amplifier to prevent large voltage swings at these nodes due to large blockers.

It should be noted that a single-ended topology is chosen for the proposed LNTA because of two reasons. First, for a differential topology a balun is required at the input, which increases the NF of the receiver at least by 1.5 dB. Moreover, due to the class-AB operation of the LNTA, its DC current increases under the large-signal condition. To avoid excessive power consumption, a single-ended topology is preferred over a differential one.

This chapter generally deals with the design and improvement of the circuit shown in Figure 3.6. Sections 3.1.1 and 3.1.2, respectively, present the input impedance and noise analysis for a HQBPF and attempt to find their LTI equivalent circuit models. The g_m, NF and selectivity of the proposed LNTA are analyzed in section 3.1.3 .

3.1.1 Analysis of the In-Band and Out-of-Band Load Impedance at V_{o1} and V_{o2}

Neglecting the nonlinear behavior of the mixer switches, the HQBPF can be considered a linear periodically time-variant (LPTV) system and can be analyzed using Fourier series. It has been shown in [34] that the HQBPF can be replaced by its LTI equivalent circuit, which will make the analysis of the LNTA much simpler. In this section, an equivalent circuit for the in-band and out-of-band frequencies is derived.

Let us consider Figure 3.7, in which the push/pull common-gate input stage is replaced by its Norton equivalent circuit, and its output impedance (the impedance looking into the drain of M_3 or M_4 when the input is terminated with the 50 Ω source impedance) is denoted by R_{out}. The equivalent parallel resistance of the LC tank is represented by R_{tank}. The capacitor of the LC tank and the effect of parasitic capacitances such as C_{gs} of M_5 and M_6 and C_{dg} and C_{db} of M_3 and M_4 are all included in C_{tot}. The parallel combination of R_{tot}, C_{tot} and L_{tank} is denoted by $Z_L(\omega)$.

[10] has proved that the RF voltage across $Z_L(\omega)$, $V_{out}(\omega)$, can be calculated through (3.1). This formula is only valid for the frequencies between $\omega_{LO}/2$ and $3\omega_{LO}/2$ and provided that $Z_{BB}(\omega)$ is zero in its stop band and the harmonics of ω_{LO} [10], which is also the case here since Z_{BB} is capacitive. Therefore, we cannot use (3.1) to evaluate how the higher harmonics of $I_{in}(\omega)$ fold and become voltage components across Z_L around ω_{LO}. In addition, (3.1) is a very good

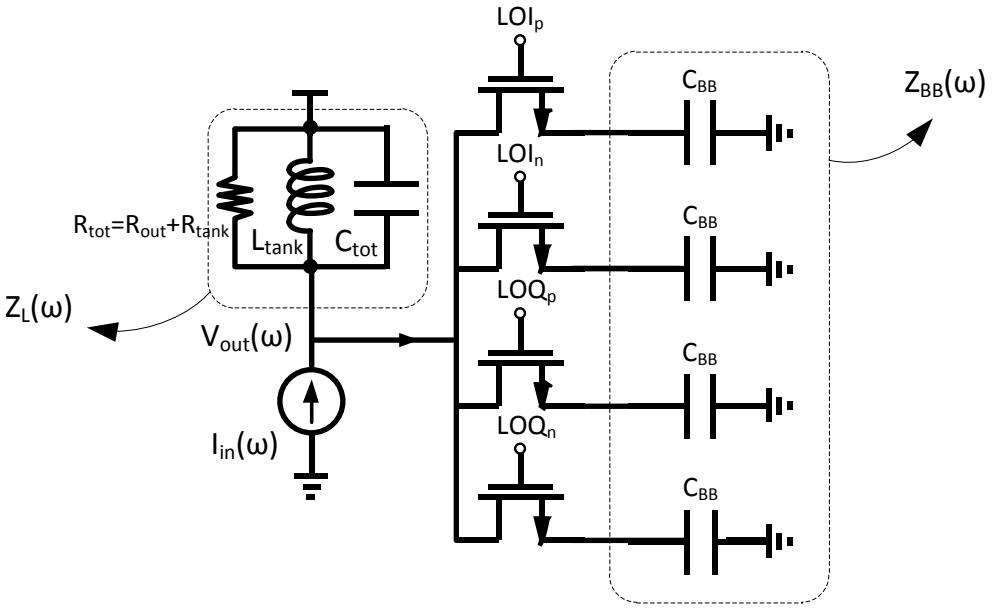


Figure 3.7: Norton equivalent circuit at the nodes v_{o1} and v_{o2} with HQBPF included.

approximation if $|Z_{BB}(k\omega_{LO})| << |Z_L(\omega_{LO})|$ (k is nonzero integer) [10], which is a valid assumption in our application.

$$\frac{V_{out}(\omega)}{I_{in}(\omega)} = R_{SW} \parallel Z_L(\omega) + \frac{\frac{2}{\pi^2}(\frac{Z_L(\omega)}{Z_L(\omega)+R_{SW}})^2 Z_{BB}(\omega-\omega_{LO})}{1+\frac{2}{\pi^2}Z_{BB}(\omega-\omega_{LO})\sum_{k=-\infty}^{+\infty}\frac{1}{(4k+1)^2[Z_L(\omega+4k\omega_{LO})+R_{SW}]}} \quad (3.1)$$

[10]

The equation of (3.1) can be simplified into (3.2) and (3.3) for close-in (in-band) and far-out (out-of-band) frequency offsets from the LO frequency, respectively. Since Z_{BB} is purely capacitive, for the close-in frequencies, we should note that it becomes very large and for far-out frequencies (although $\omega_{LO}/2<\omega$ and $\omega<3\omega_{LO}/2$ for (3.1) to be valid), it becomes negligible.

$$\frac{V_{out}(\omega)}{I_{in}(\omega)} \approx R_{SW} \parallel Z_L(\omega) + \frac{(\frac{Z_L(\omega)}{Z_L(\omega)+R_{SW}})^2}{\sum_{k=-\infty}^{+\infty}\frac{1}{(4k+1)^2[Z_L(\omega+4k\omega_{LO})+R_{SW}]}} \quad (3.2)$$

[10]

$$\frac{V_{out}(\omega)}{I_{in}(\omega)} \approx R_{SW} \parallel Z_L(\omega) \quad (3.3)$$

Since Z_L is a tuned RLC load and R_{tot} is large, we can assume that $R_{SW} << Z_L(\omega_{LO})$ and simplify (3.2) to (3.4).

$$Z_{in-band}(\omega) \approx R_{SW} + \frac{1}{\sum_{k=-\infty}^{+\infty}\frac{1}{(4k+1)^2[Z_L(\omega+4k\omega_{LO})+R_{SW}]}} \quad (3.4)$$

By rewriting (3.4) we get

$$Z_{in-band}(\omega) = R_{SW} + \frac{1}{\frac{1}{Z_L(\omega)+R_{SW}} + \sum_{k=-\infty,k\neq 0}^{+\infty}\frac{1}{(4k+1)^2[Z_L(\omega+4k\omega_{LO})+R_{SW}]}} \quad (3.5)$$

Using a similar approach to [34], we can now find the LTI equivalent circuit of the HQBPF for the in-band frequencies, shown in Figure 3.8, by inspecting (3.5). This circuit model can be used for calculation of the in-band gain of the LNTA, but it cannot be used for noise analysis, since it does not consider the folding of higher harmonics of $I_{in}(\omega)$, as mentioned earlier.

In Figure 3.8, the *virtual* impedance $Z_v(\omega)$ represents the loss due to the harmonic

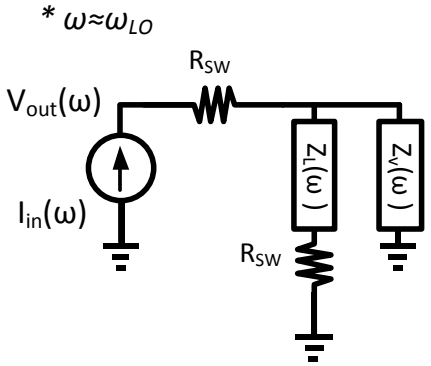


Figure 3.8: LTI in-band equivalent circuit model (similar to [34]) for the HQBPF with parallel load Z_L.

reupconversion [34] and can be written as (3.6).

$$Z_v(\omega) = \left(\sum_{k=-\infty, k\neq 0}^{k=+\infty} \frac{1}{(4k+1)^2 [Z_L(\omega + 4k\omega_{LO}) + R_{SW}]} \right)^{-1} \tag{3.6}$$

For the special case where Z_L is resistive and equal to R_{tot}, the equivalent in-band impedance becomes [10]

$$Z_{in-band}(\omega) = R_{SW} + \frac{8}{\pi^2}(R_{tot} + R_{SW}) \tag{3.7}$$

For our case where Z_L is an RLC tank, such a closed-form equation cannot be found, although through the mathematical manipulations, explained below, we try to make (3.5) more intuitive and useful for our design:

The RLC tank impedance, when tuned to ω_{LO}, can be written as in (3.8), where Q denotes the quality factor of the tank and is defined in (3.9). Now by substituting (3.8) into (3.6), and noting that $\omega=\omega_{LO}$ for in-band frequencies we get (3.10), where γ is given by (3.11).

$$Z_L(\omega) = \frac{R_{tot}}{Q} \frac{j\omega / \omega_{LO}}{1 + j\frac{\omega}{Q\omega_{LO}} - (\frac{\omega}{\omega_{LO}})^2} \tag{3.8}$$

$$Q = \frac{R_{tot}}{\omega_{LO} L} \tag{3.9}$$

$$Z_v(\omega \approx \omega_{LO}) = \gamma R_{tot} \tag{3.10}$$

$$\gamma = (\sum_{k \neq 0} \frac{1}{(4k+1)^2 \left[\frac{1}{Q} \cdot \frac{j(4k+1)}{1 + j\frac{4k+1}{Q} - (4k+1)^2} + \frac{R_{SW}}{R_{tot}} \right]})^{-1} \tag{3.11}$$

According to the equivalent circuit of Figure 3.8 and using (3.10), the in-band input impedance of the circuit shown in Figure 3.7 can be written as (3.12), assuming $R_{SW} << R_{tot}$.

$$Z_{in-band}(\omega \approx \omega_{LO}) \approx \beta \cdot R_{tot} + R_{SW} \tag{3.12}$$

where

$$\beta(Q, \frac{R_{SW}}{R_{tot}}) = \frac{\gamma}{1+\gamma} \tag{3.13}$$

The coefficient β can be calculated using mathematical software such as MATLAB for different values of R_{SW}/R_{tot}, and Q. A special case, where Z_L is purely resistive, we can assume $Q << 1$. This leads to $\beta \approx 0.81 \approx \frac{8}{\pi^2}$, which is also proved by (3.7).

Shown in Figure 3.9 is the magnitude of β for different values of Q with R_{SW}=10 Ω. We can see that as the quality factor of the tank reduces, β (hence, $Z_{in\text{-}band}$) increases; however, this is not readily seen from (3.5). In other words, the lower the selectivity of the RLC tank, the higher the in-band impedance of the filter.

It will be shown in section 3.1.33.1.3 that the gain and the noise of the proposed LNTA improve as the in-band impedance of the HQBPFs increases, suggesting that the Q-factor of the RLC tank should not be necessarily large. This is desirable since the inductor of the RLC tank, which is the most area consuming component, can be made as compact as possible.

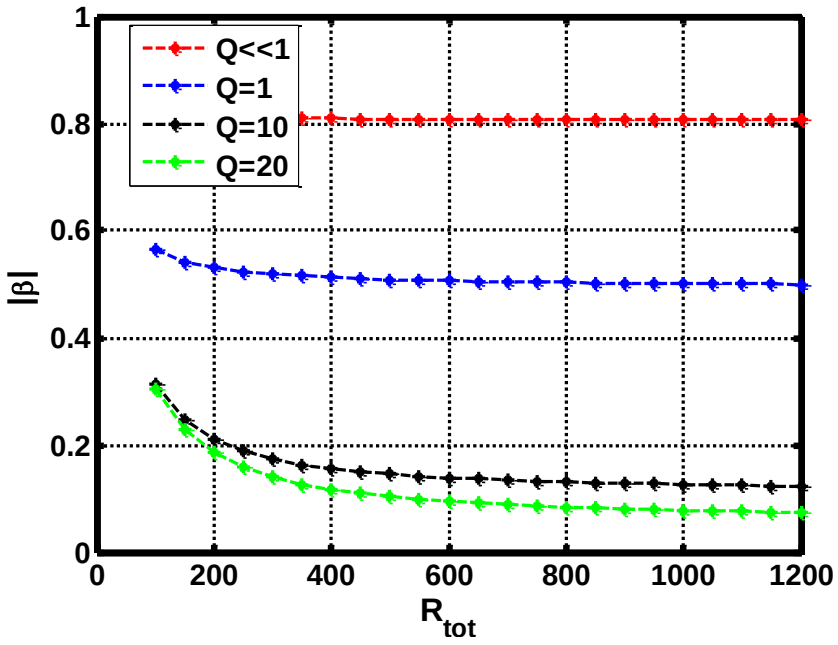


Figure 3.9: |β| for various values of RLC tank Q-factor (R_{SW}=10Ω).

To investigate the effect of R_{SW} on the in-band impedance, β versus R_{tot} for various values of R_{SW} and Q is plotted in Figure 3.10. It can be seen that R_{SW} does not have any significant effect on |β| for small values of Q. But for higher values of Q (e.g. Q=10), which are more practical here, by doubling R_{SW}, |β| increases roughly by 66%. According to (3.12), this can significantly improve $Z_{in\text{-}band}$.

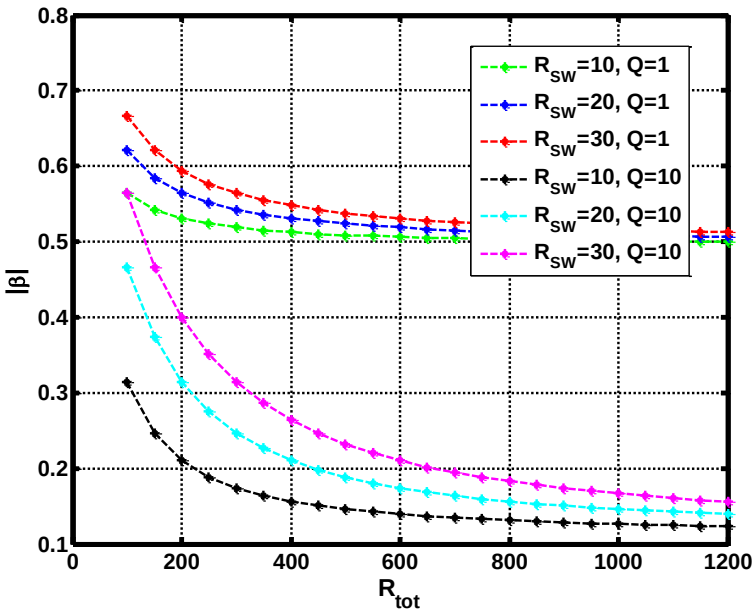


Figure 3.10: |β| for various values of R_{SW} and Q.

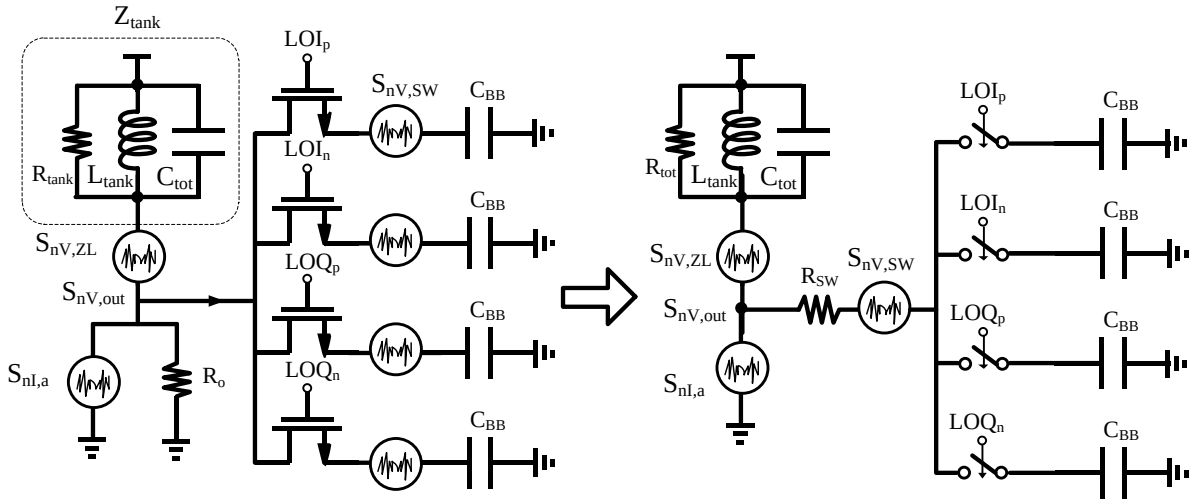
So far we have derived the LTI equivalent circuit model for the HQBFPs used in parallel with an RLC tank as shown in Figure 3.6. In addition, it was pointed out that the equivalent circuit is not valid for noise analysis and nor does provide us with the information how the higher harmonics of $I_{in}(\omega)$ are folded back across Z_L around ω_{LO}. Therefore, the effect of harmonic conversion on the noise is accounted for in the next section.

3.1.2 Analysis of the On-Chip High-Q Bandpass Filter Noise[4]

Analyzing the noise of the HQBPF is tricky since, unlike the input impedance of the HQBPF that can be simply replaced by its LTI equivalent impedance around ω_{LO} (in-band frequencies), for noise analysis this simplification is no longer true.

To understand how the HQBPF contributes to the noise of the LNTA, consider Figure 3.11. In this figure, $S_{nV,SW}$ denotes the single-sided voltage noise PSD of the switches, which is equal to $4kTR_{SW}$. The noise contribution of the input transistors M_1 to M_4 and R_s (see Figure 3.6) is designated as $S_{nI,a}$, and the Thévenin equivalent noise source of the RLC tank (S_{nV,Z_L}) is given by

$$S_{nV,Z_L} = 4kT \cdot re\{Z_{tank}\} \tag{3.14}$$



(a) (b)

Figure 3.11: (a) Distribution of the noise sources. (b) Equivalent circuit with a series and a parallel noise source representing all the noise sources in the circuit.

[4] Hereinafter, S_{nV} and S_{nI} denote the single-sided voltage and current noise PSD, respectively

According to [10], since the thermal noise of the switches do not have any correlation and the clock signals are non-overlapped, the HQBPF can be replaced by its equivalent circuit shown in Figure 3.11 (b), where switches are ideal (R_{SW}=0 and noiseless).

Because the HQBPF is a linear-time-variant (LTV) system, it can fold back the noise around the higher harmonics of ω_{LO} to ω_{LO}. [10] has derived the gain by which the frequency components of $S_{nV,SW}$ around the odd[5] order harmonics of ω_{LO} fold back and become voltage across Z_L. By using (3.6), the gain can be written as

$$G_{4k+1,SW} = \begin{cases} \dfrac{Z_v(\omega_{LO}) \| [Z_L(\omega_{LO}) + R_{SW}]}{Z_v(\omega_{LO})}; & k = 0 \\ Z_v(\omega_{LO}) \| [Z_L(\omega_{LO}) + R_{SW}] \times \dfrac{(-1)^k}{(4k+1)\{Z_L[(4k+1)\omega_{LO}] + R_{SW}\}}; & k \neq 0 \end{cases} \quad (3.15)$$

[10]

According to (3.15) and the simplified circuit of Figure 3.11 (b), the noise voltage PSD at ω_{LO} and across Z_L due to the thermal noise of the switches ($S_{nV,out,SW}$) is now given by

$$S_{nV,out,SW} = S_{nV,SW} \times \sum_{k=-\infty}^{+\infty} |G_{4k+1,SW}|^2 \qquad V^2/Hz \quad (3.16)$$

[10]

By working out (3.16), it has been shown in [10] that for a purely restive load (R_L), provided that $R_{SW} << R_L$, the noise contribution of the switches is negligible compared to the noise contribution of R_L. It will be shown that for an RLC load this is not generally the case and for Q>>1, the switches are the main source of the noise.

Now, let us aim to find the output voltage noise PSD ($S_{nV,out}$) in case of an RLC load. To do this, we need the gain by which the frequency components of $S_{nI,tot}$ around the odd order harmonics of ω_{LO} fold back and become noise voltage across Z_L around ω_{LO}. The approach employed here is partly similar to [34], where the LTI equivalent circuit is also used for noise calculations; although our approach is more general.

[5] Due to the differential structure of the HQBPF, frequency components at the even order harmonics of the input current signal or the switches noise source do not contribute to any voltage across Z_L [10].

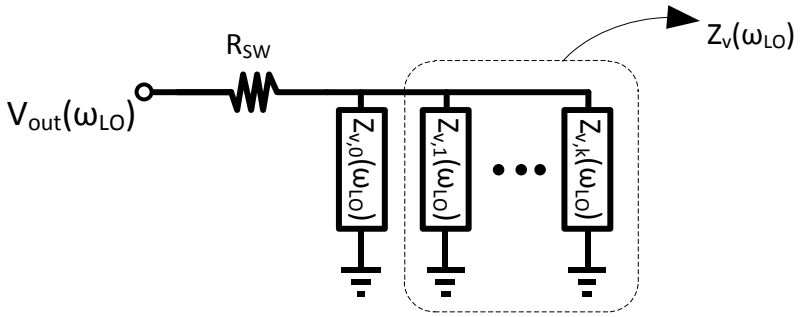


Figure 3.12: Modified LTI equivalent circuit of the HQBPF.

For our discussions we use the LTI equivalent circuit of Figure 3.8 with slight modification as shown in Figure 3.12, where $Z_{v,k}(\omega_{LO})$ is defined as (3.17), which denotes the components of the virtual impedance $Z_v(\omega_{LO})$. $Z_v(\omega_{LO})$ is now redefined as in (3.18), which from the equivalent circuit point of view can be represented by the circuit illustrated in Figure 3.12.

$$Z_{v,k}(\omega_{LO}) = (4k+1)^2[Z_L((4k+1)\omega_{LO}) + R_{SW}] \tag{3.17}$$

$$Z_v(\omega_{LO}) = \frac{1}{\sum_{k\neq 0}\frac{1}{Z_{v,k}(\omega_{LO})}} \tag{3.18}$$

[34]

As shown in Figure 3.13 (a), using the Thévenin theorem, we can convert the parallel input current to an equivalent voltage source ($V_{th}(\omega)$) in series with Z_L, or $V_{th}(\omega)$ can represent the thermal noise of Z_L. For a wideband noise current source at the input with PSD of $S_{nI,a}$ and for the thermal noise of Z_L, $V_{th}(\omega)$ is given by (3.19) and (3.20), respectively.

$$V_{th}^2(\omega) = |Z_L(\omega)|^2 \times S_{nI,a} \tag{3.19}$$

$$V_{th}^2(\omega) = 4kT \cdot re\{Z_L(\omega)\} \tag{3.20}$$

By combining the two approaches explained in [34] and [10] and using the LTI model of Figure 3.13 (b) , we can now find the voltage gain, which is given by (3.21), from $(4k+1)$ harmonic of $V_{th}(\omega)$ to $V_{out}(\omega)$ around ω_{LO}.

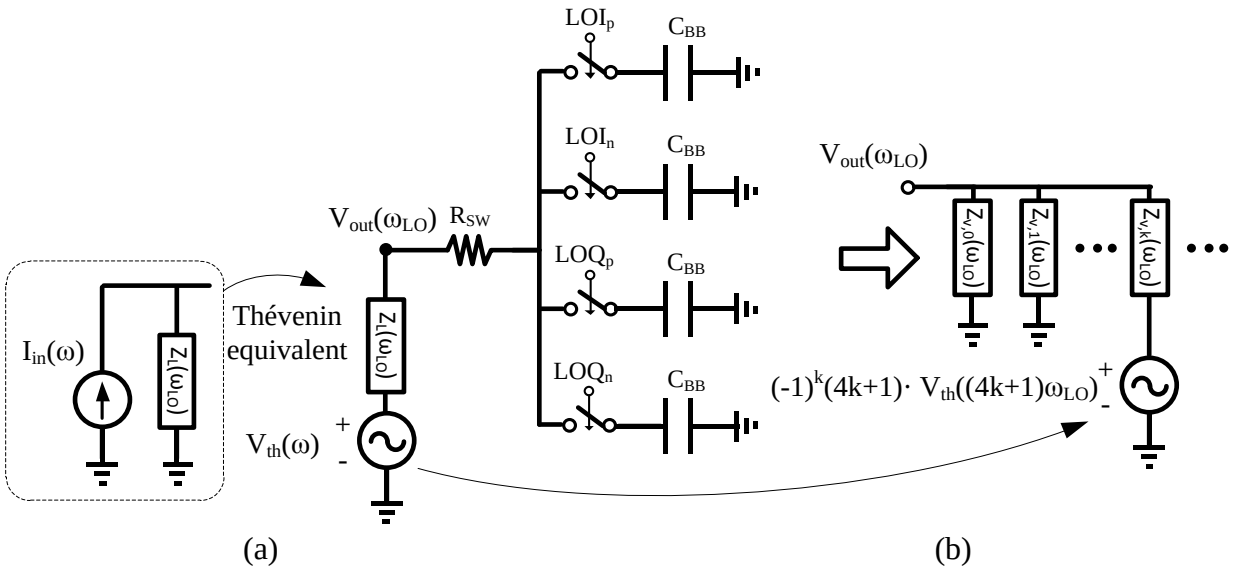


Figure 3.13: (a) Thévenin equivalent of the input current source. (b) Equivalent LTI model to calculate the gain from $(4k+1)$ harmonic of $V_{th}(\omega)$ to $V_{out}(\omega)$ around ω_{LO}.

$$G_{4k+1,th} = \frac{V_{out}(\omega_{LO})}{V_{th}((4k+1)\omega_{LO})} \approx \begin{cases} \dfrac{\beta R_{tot} + R_{sw}}{R_{tot}}; & k = 0 \\ \dfrac{(-1)^k (4k+1)}{Z_{v,k}(\omega_{LO})} \times \beta R_{tot}; & k \neq 0 \end{cases} \tag{3.21}$$

By substituting (3.19) and (3.20) into (3.22), the output noise is given by (3.23) and (3.24) for the noisy load impedance (Z_L) and the wideband input noise, respectively. And to calculate the in-band noise arising from the thermal noise of the switches, we should use (3.16). Finally, the output noise voltage due to all the noise sources can be calculated through (3.25).

$$S_{nV,out} = \sum_{k=-\infty}^{+\infty} |G_{4k+1,th}|^2 \, V_{th}^2((4k+1)\omega_{LO}) \tag{3.22}$$

$$S_{nV,out,Z_L} = 4kT \sum_{k=-\infty}^{+\infty} |G_{4k+1,th}|^2 \, re\{Z_L((4k+1)\omega_{LO})\} \tag{3.23}$$

$$S_{nV,out,Ia} \approx (|\beta| R_{tot})^2 \times \tfrac{\pi^2}{8} \times S_{nI,a} \tag{3.24}$$

$$S_{nV,out} = S_{nV,out,Ia} + S_{nV,out,sw} + S_{nV,out,Z_L} \tag{3.25}$$

By assuming a purely resistive load (Q<<1, $R_{tot} = R_L$, and $S_{nI,a} = 4kT/R_L$) and considering only its thermal noise, from (3.13) we can calculate $\beta = \frac{8}{\pi^2}$, and (3.24) simplifies to (3.26), which is also verified by [10] and the simulations.

$$S_{nV,out,R_L} = 4kTR_L(8/\pi^2) \tag{3.26}$$

To further verify (3.25), we have performed simulations (PSS+PNOISE in Spectre RF) for various values of Q and R_{tot} assuming $S_{nI,a} = 4kT \cdot 10^{-2}$ for the circuit shown in Figure 3.14 and compared the results to (3.25). The results are shown in Table 3.1. From this table we can see that the predicted and the simulated results well agree.

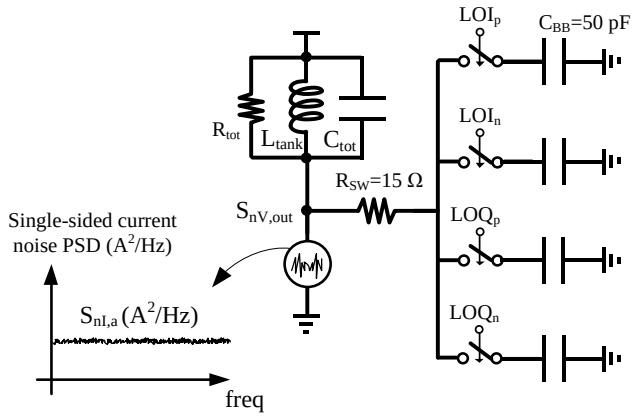


Figure 3.14: Schematic used for simulations and "hand-calculations".

Q	R_{tot} (kΩ)	predicted/simulated $\frac{S_{nV,out,sw} + S_{nV,out,Z_L}}{4kT}$	predicted/simulated $\frac{S_{nV,out,Ia}}{4kT}$
1	1	522/380	3146/3120
10	0.5	97.2/90.5	85.4/98
10	1	148/135	228/257
20	0.5	80.2/74.9	52.9/63
20	1	103/99.5	101/121

Table 3.1: Comparison of the simulated (PSS+PNOISE in Spectre RF) and the predicted [equation (3.25)] voltage noise at the input of the HQBPF (R_{SW}=15 Ω).

3.1.3 Analysis of the LNTA NF, Transconductance, and Selectivity

The previous two sections provided us with LTI equivalent circuits for noise and input impedance analysis of the HQBPFs in parallel with an RLC tank. These equivalent circuits can now be readily used to calculate the noise figure and the transconductance of the proposed LNTA. The simplified schematic for the analysis of LNTA input impedance and transconductance (g_{mLNTA}) is shown in Figure 3.15. For sake of simplicity, it is assumed that the operating frequency is well below f_T meaning that C_{ds} of all transistors, and the drain parasitic capacitances of M_1, M_2, M_5 and M_6 can be neglected. Furthermore, since L_s is chosen to resonate out with the parasitic capacitances of the input node, it is safe to neglect L_s and the parasitic capacitances on node V_{in} in the analyses of this section.

The HQBPF is also substituted by its LTI equivalent circuit model $Z_{eqv}(\omega)$, which according to the analysis of section 3.1.1 is given by (3.12) and (3.3) for in-band and out-of-band frequencies, respectively, and are repeated here in (3.27) for sake of convenience. The input impedance can be calculated using the schematic of Figure 3.16 showing the small-signal equivalent circuit of

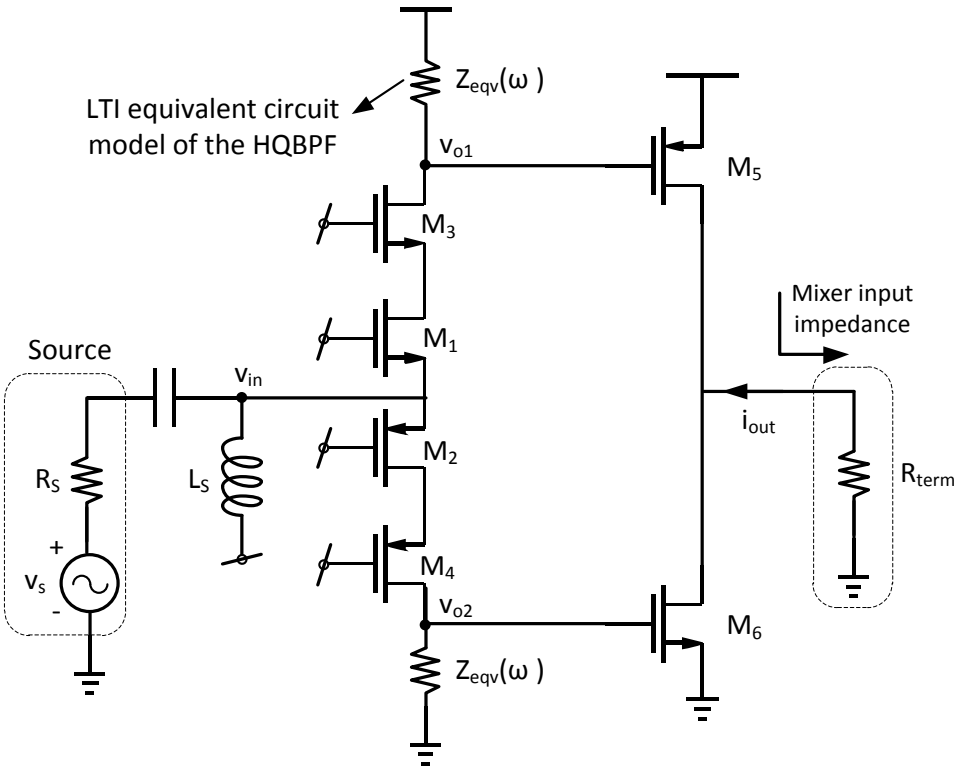


Figure 3.15: Simplified schematic for transconductance analysis.

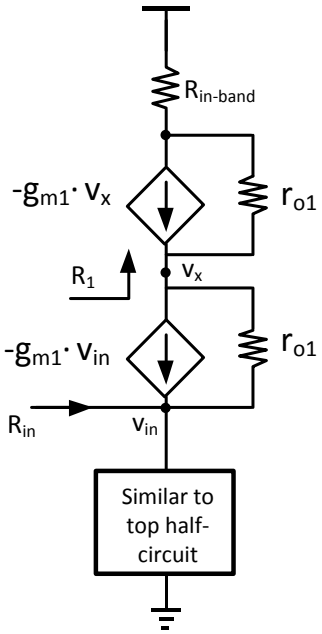


Figure 3.16: Small-signal schematic of the top half-circuit for the input impedance analysis.

Figure 3.15, assuming equal transconductance (g_{m1}) and drain-source resistance (r_{o1}) for the transistors M_1 to M_4[6]. The input impedance can be simplified as (3.28) [35].

$$Z_{eqv}(\omega) \approx \begin{cases} \beta R_{tot} + R_{sw} & : R_{in-band}(\omega \approx \omega_{LO}) \\ R_{sw} & : out-of-band \end{cases} \tag{3.27}$$

$$R_{in} = \frac{1}{2}\frac{r_{o1}+R_1}{1+g_{m1}r_{o1}} = \frac{1}{2}\frac{r_{o1}+\frac{r_{o1}+R_{in-band}}{1+g_{m1}r_{o1}}}{1+g_{m1}r_{o1}} = \frac{1}{2}\frac{2r_{o1}+g_{m1}r_{o1}^2+R_{in-band}}{(1+g_{m1}r_{o1})^2} \tag{3.28}$$

For the special case where $g_{m1}r_{o1} >> R_{eq} >> 1$, R_{in} is simplified to

$$R_{in} \approx \frac{1}{2 \cdot g_{m1}} \tag{3.29}$$

From (3.29), we can see that for 50 Ω input impedance matching, g_{m1} should be around 10 mS. For the desired operating point we could see that the assumption of $g_{m1}r_{o1} >> R_{eq}$ is no longer true, and (3.28) should be used for accurate calculation of the input impedance.

[6] Although g_m for the PMOS and NMOS transistor can be made equal through proper sizing, we cannot have control over its r_o (with a fixed channel length and current). Here, we have ignored this to make the formulae compact.

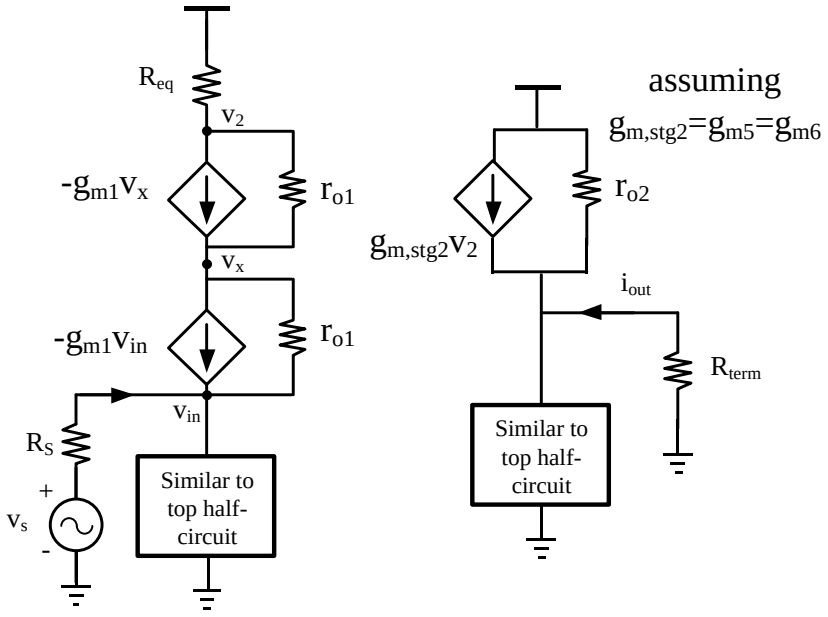


Figure 3.17: Small-signal schematic used for g_{mLNTA} derivation.

To calculate g_{mLNTA}, which is defined as (3.30), the schematic of Figure 3.17 is used. It is also assumed here that the transistors of the second stage (M_5 and M_6 in Figure 3.15) have equal g_m and r_o. Since $r_{o2} >> R_{term} (\approx 10\Omega)$, in-band (IB) g_{mLNTA} can simply be written as (3.31).

$$g_{mLNTA} = \frac{i_{out}}{v_{in}} \tag{3.30}$$

$$g_{mLNTA,IB} \approx \frac{g_{m,stg2} R_{in-band}}{R_{in}} \text{ (assuming } r_{o2} >> 2 \cdot R_{term}) \tag{3.31}$$

By comparing (3.31) to the transconductance of the single stage push/pull common-gate amplifier, it can be noticed that g_m has increased by a factor of $g_{m,stg2} R_{in-band}$. Out-of-band (OB) g_m can also be derived following similar steps as above. The result is given by (3.32), where $R_{in,OB}$ is equal to (3.33).

$$g_{mLNTA,OB} \approx \frac{g_{m,stg2} R_{sw}}{R_{in,OB}} \tag{3.32}$$

$$R_{in,OB} = \frac{1}{2} \frac{2r_{o1} + g_{m1} r_{o1}^2 + R_{sw}}{(1 + g_{m1} r_{o1})^2} \approx \frac{1}{2} \frac{2r_{o1} + g_{m1} r_{o1}^2}{(1 + g_{m1} r_{o1})^2} \tag{3.33}$$

Having both $g_{mLNTA,OB}$ and $g_{mLNTA,IB}$, we can now define selectivity as (3.34), which quantifies the dynamic range of the RF filtering by the LNTA. It can be inferred that the higher the selectivity, the lower the blocker-induced current-swing at the output of the LNTA and through the mixer. This can significantly relax the linearity and the noise performance of the mixer, by reducing LO re-mix and disturbance in the switching behavior of the downconversion passive current mixer [24].

$$Selectivity = 20\log(\frac{g_{mLNTA,IB}}{g_{mLNTA,OB}}) \tag{3.34}$$

In order to find a design equation for the NF of the LNTA, the thermal noise of the transistors, Z_L, and high-Q bandpass filters are incorporated in the LTI equivalent circuit model of Figure 3.18. To simplify the analysis, the noise contribution of the cascode devices (M_3 and M_4) is neglected here, since they are partially cancelled due to r_o of the transistors. The noise current due to drain noise is denoted by $\overline{i_{nd}^2}$ and is equal to $4kT\gamma g_m$ [35], where γ is fitting parameter of

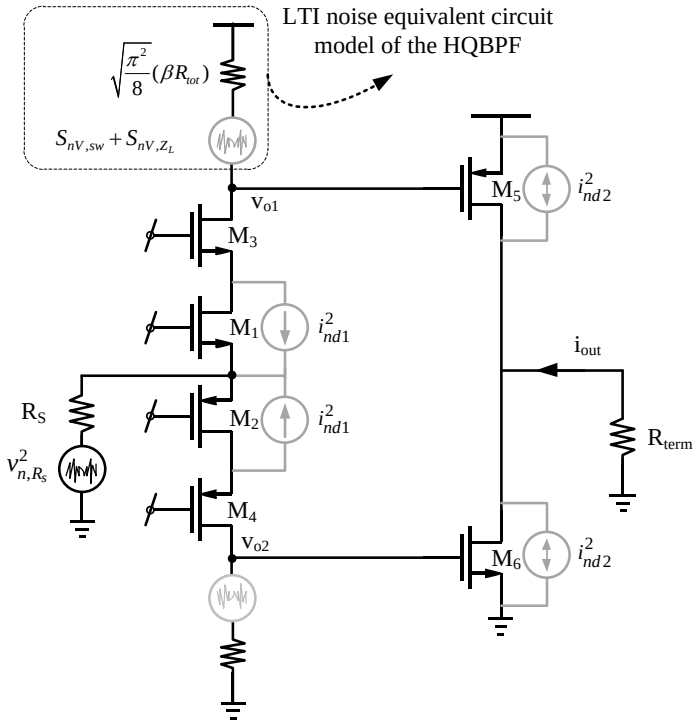


Figure 3.18: LTI noise equivalent circuit model of the LNTA.

the noise model, and for short channel devices reports of γ=1 [29] or γ=1.45 [28] exists in the literature.

To calculate the NF, we should be careful since the LTI circuit models used for the signal gain and noise analysis are different. According to the definition of noise factor, which is equal to $\frac{SNR_{in}}{SNR_{out}}$ [35], we need to find the in-band output current noise ($S_{nI,out,tot}$) due to all the noise sources (including R_s) using the circuit of Figure 3.18. However, to refer the thermal noise of R_s to the output (S_{nI,out,R_s}), we need to use the *in-band* signal gain, which is given by (3.30). This unconventional approach stems from the fact that HQBPF is an LTV system. In the contrary to LTI systems, we cannot define a single gain for both noise and the signal.

Now by substituting $S_{nI,out,tot}$ and S_{nI,out,R_s} from (3.35) and (3.36), respectively, into noise factor definition, we can find noise factor using (3.37). In the derivation of (3.37), it is assumed that LNTA is power matched at its input ($R_{in} = R_s$) and $R_{in} \approx \frac{1}{2g_{m1}}$.

$$S_{nI,out,tot} = \frac{\pi^2}{8}(\beta R_{tot} g_{m,stg2})^2 \frac{i_{nd1}^2}{2} + 2i_{nd2}^2 + 2(S_{nV,Z_L} + S_{nV,sw}) g_{m,stg2}^2 + \frac{\pi^2}{8}(\frac{\beta R_{tot} g_{m,stg2}}{R_{in}})^2 \frac{S_{nV,R_s}}{4} \quad (3.35)$$

$$S_{nI,out,R_s} = (g_{mLNTA,IB})^2 \frac{S_{nV,R_s}}{4} \quad (3.36)$$

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{nI,out,tot}}{S_{nI,out,R_s}} \approx \frac{\pi^2}{8}(\frac{\beta R_{tot}}{R_{in-band}})^2 (1+\gamma_{stg1}) + \frac{8R_{in}}{R_{in-band}^2}(\frac{S_{nV,Z_L} + S_{nV,sw}}{4kT} + \gamma_{stg2}) \quad (3.37)$$

From (3.37) it can be concluded that to minimize NF, $R_{in-band}$ should be as large as possible. In addition, the effect of the second stage transconductance, $g_{m,stg2}$ on NF becomes trivial provided that $8R_S << R_{in-band}^2$, which is the case in our design.

3.1.4 The Impact of High-Q Bandpass Filters on the Large-Signal Behavior of the LNTA

As explained in section 3.1, the large-signal behavior of the push/pull common-gate stage strongly depends on its load impedance or, equivalently, its drain voltage swing; and for large load impedances the amplifier can no longer operate in class-AB mode. One advantage of using the HQBPFs as load impedances is that they can provide low out-of-band impedances, hence improving the linearity of the common-gate stage. However, large blockers lead to large current swings through the HQBPFs that might perturb the normal operation of the filters. Therefore, it is necessary to study their large signal behavior and ensure a reliable operation.

At the presence of a large blocker, large current flows into the common-gate amplifier. For sufficiently large blockers, we can assume that, due to the push/pull property of the amplifier, the blocker current only flows through either the PMOS or the NMOS transistor. As an example, consider a continuous-wave (CW) +10 dBm blocker at 100 MHz offset frequency from the wanted signal. It can be calculated from (3.38) that this blocker causes +20 mA peak current swing (assuming 50Ω input impedance) at the input, which, depending on the phase of the CW

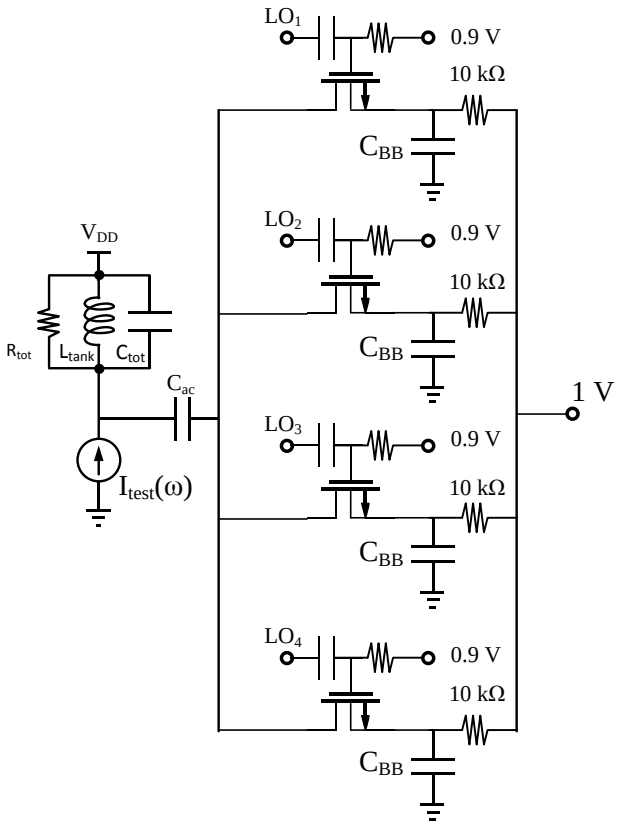


Figure 3.19: Simulation test-bench to study the large-signal behavior of the HQBPFs.

signal, flows into the top or bottom branch. Although the HQBPF filters this blocker current and prevents large voltage swing at the output of the common-gate amplifier, they should still be able to tolerate this current swing.

$$20\log(I_{in})[dBmA_{peak}] = P_{in}[dBm] - 10\log(R_{in}/2) - 30dB \approx P_{in}[dBm] - 44(dB) \qquad (3.38)$$

The HQBPF is in general an NLTV system and, in case of weak nonlinearity (higher than 3rd order nonlinear terms are ignored) behavior, Volterra series can be used to analyze its distortion similar to [36]. However, performing such analysis is out of the scope of this work due to the complications of the Volterra series analysis for time-varying systems [31]. In addition, here the large-signal behavior of the HQBPF is of concern rather than its small-signal distortion behavior. Therefore, an intuitive approach based on the simulations is adopted here.

The circuit shown in Figure 3.19 is used to investigate the in-band impedance of the HQBPF at the presence of a large blocker. For the purpose of the simulation, an ideal 25% duty-cycle clock generator with rise/fall time of $30p\,\text{sec}$ was used. The size of the transistors was chosen in such

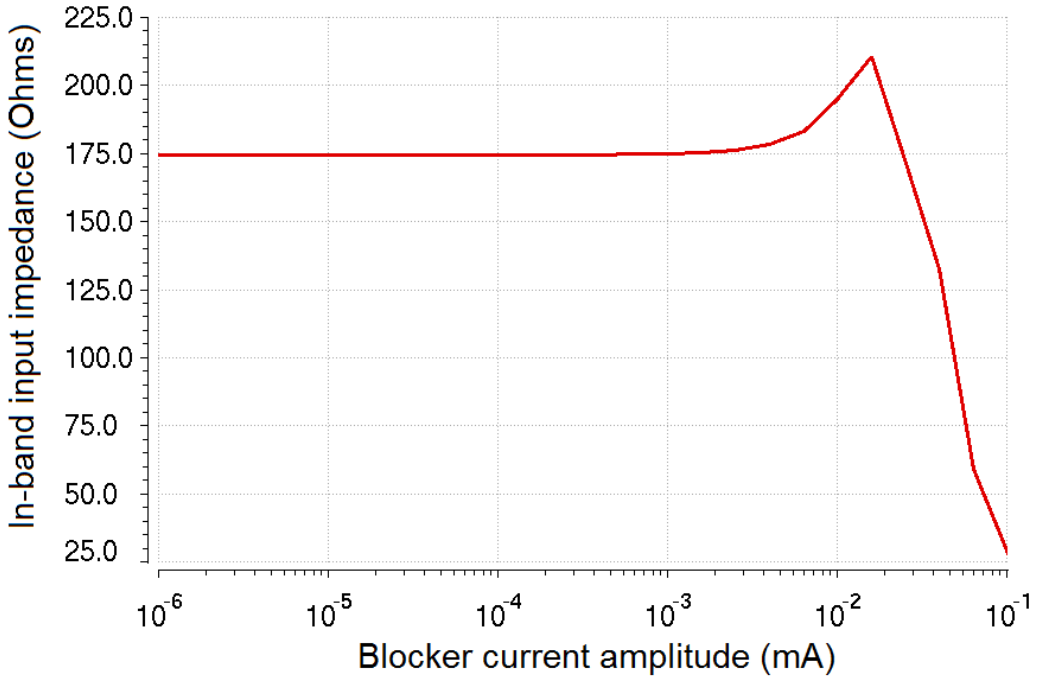


Figure 3.20: In-band input impedance of the HQBPF versus the current amplitude of an out-of-band CW blocker.

way to result in $R_{sw} = 33\Omega$, and the rest of the circuit parameters were as follows: $R_{tot} \approx 570\Omega, L_{tank} = 4nH, \omega_0 \approx 2GHz, C_{BB} = 20pF$. Using PSS+PAC analysis, the small-signal input impedance was found at the presence of a CW out-of-band (100 MHz offset) blocker while sweeping the blocker current amplitude. The results are plotted in Figure 3.20. Interestingly, it can be seen that the value of the input impedance expands to some extent for current amplitude of around 20 mA. This feature can be exploited to compensate for the (V-to-I conversion) gain compression of the input common-gate stage. This, accordingly, helps to improve the compression point of the LNTA.

3.2 NF Improvement Using CG/CS Noise Cancellation Technique

Figure 3.21 shows the simplified schematic of the proposed LNTA incorporating an auxiliary g_m path for noise-cancellation and g_m-enhancement. Similar to the circuit proposed by [33], the LNTA consists of a main path, which provides input 50 Ω matching, and an auxiliary path (M_7 and M_8), which enables noise cancellation and g_m-enhancement. However, the LNTA proposed in Figure 3.21 differs from the combined CG/CS architecture of [33] due to the use of linearizing cascode transistors (M_3 and M_4).

Furthermore, in contratry to [33] and [37], in this work the push/pull property of the LNTA is maintained by implementing all the stages using complementary NMOS/PMOS transistors. In this way, complementary characteristics of NMOS and PMOS transistors are utilized to improve the small-signal (IIP2 and IIP3) as well as large-signal linearity (P_{1dB}) [29]. In addition, the auxiliary CS stage bias is tuned for class-AB operation under large signal conditions. As a result of the push/pull class-AB operation of both the CG and CS stages, the LNTA becomes capable of handling larger signals at reduced bias current.

[29] has similarly employed push/pull CG and CS stages, with the CS stage operating as a class-

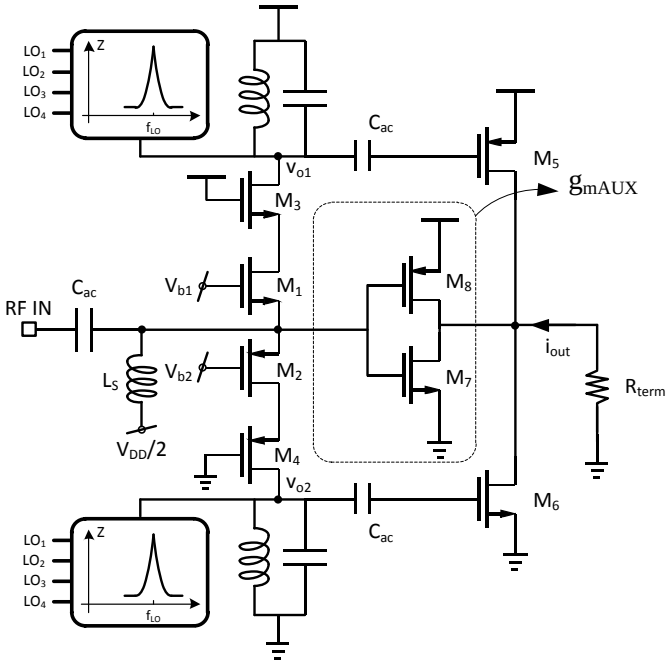


Figure 3.21: The simplified schematic of the proposed LNTA incorporating the auxiliary path.

AB amplifier. In [29], the output current of the CG stage is added with the CS stage current through resistive current dividers in a fully differential cross-coupled fashion to inverse the polarity of the CS stage current. To accommodate for the dc voltage drop of the resistive current dividers, a relatively high supply voltage of 2.2 V is employed. Using the push/pull combined CS/CG topology, [29] has reported a 0 dBm compression point and an IIP3 of +10.8 dBm for a fully differential structure.

The principle behind the noise cancellation technique used by [33] or [38] is a straight forward idea: the noise appearing at the input of the amplifier due to the input transistors providing wide-band 50 Ω matching is cancelled at the output through an auxiliary feed-forward path. The desired signal reaches to the output with the same phase through the main and the auxiliary path; hence the g_m of the LNTA is also effectively enhanced, while the noise reaches to the output through the auxiliary path with 180° phase shift and gets cancelled.

In the following sections, the g_m and the NF of the proposed LNTA of Figure 3.21 are analyzed in a similar way to section 3.1.3. Section 3.2.2 provides a rather intuitive discussion on the large-signal behavior of the auxiliary CS stage and explains how the linearity can be enhanced through class-AB operation.

3.2.1 Noise, Gain, and Selectivity Analysis

To show the noise cancelling and g_m-enhancement feature of the LNTA shown in Figure 3.21, its NF and g_m are analyzed in this section in a similar fashion as section 3.1.3. For the small-signal analyses of this section it is assumed that $g_{m7} = g_{m8}$ and the input parasitic capacitance (mostly due to C_{gs} of M_1, M_2, M_7 and M_8) resonates out with L_s.

The in-band and out-of-band g_m of the LNTA are now given by (3.39) and (3.40), respectively, where g_{mAUX} denotes the combined transconductance of the auxiliary path and is equal to $g_{m7} + g_{m8}$. From (3.39) and (3.40) we can see that, although by increasing g_{mAUX} we can achieve more g_m-enhancement, the selectivity of the LNTA also reduces due to higher $g_{mLNTA,OB}$. For the extreme case that $\frac{g_{m,stg2}\,\mathrm{R}_{in-band}}{R_{in}} << g_{mAUX}$, LNTA g_m is dominated by g_{mAUX}; hence, no selectivity.

$$g_{mLNTA,IB} \approx \frac{g_{m,stg2}\,\mathrm{R}_{in-band}}{R_{in}} + g_{mAUX} \quad (\text{assuming } r_o >> 4\cdot \mathrm{R}_{term}) \tag{3.39}$$

$$g_{mLNTA,OB} \approx \frac{g_{m,stg2}\,\mathrm{R}_{sw}}{R_{in,OB}} + g_{mAUX} \tag{3.40}$$

To calculate the noise factor, (3.35) and (3.36) can be used with slight modification to incorporate the noise ($i^2_{nd,aux}$) and g_{mAUX} of the auxiliary path. For the LNTA of Figure 3.21, $S_{nI,out,tot}$ and S_{nI,out,R_s} can be calculated through (3.41) and (3.42), respectively, where $g_{mLNTA,IB}$ is now given by (3.39). It can be seen from the first term of (3.43) that by proper choice of g_{mAUX} and $g_{m,stg2}$, the noise arising from the input CG stage can be cancelled.

$$\begin{aligned} S_{nI,out,tot} &= (R_{in}g_{mAUX} - \sqrt{\frac{\pi^2}{8}}\beta R_{tot}g_{m,stg2})^2\,\frac{i^2_{nd1}}{2} + 2i^2_{nd2} + 2(S_{nV,Z_L} + S_{nV,sw})g^2_{m,stg2} \\ &+ (\frac{\sqrt{\frac{\pi^2}{8}}\beta R_{tot}g_{m,stg2}}{R_{in}} + g_{mAUX})^2\,\frac{S_{nV,R_s}}{4} + 2i^2_{nd,aux} \end{aligned} \tag{3.41}$$

$$S_{nI,out,R_s} = (g_{mLNTA,IB})^2 \frac{S_{nV,R_s}}{4} \tag{3.42}$$

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{nI,out,tot}}{S_{nI,out,R_s}} \approx \left(\frac{g_{mAUX} - \sqrt{\frac{\pi^2}{8}} \frac{\beta R_{tot} g_{m,stg2}}{R_{in}}}{g_{mAUX} + \frac{R_{in-band} g_{m,stg2}}{R_{in}}} \right)^2 \gamma_{stg1} + \left(\frac{1}{g_{mAUX} + \frac{R_{in-band} g_{m,stg2}}{R_{in}}} \right)^2 \frac{4 g_{mAUX}}{R_{in}} \gamma_{aux} + \ldots \tag{3.43}$$

According to (3.43) to minimize noise factor $g_{mAUX} = \sqrt{\frac{\pi^2}{8}} \frac{\beta R_{tot} g_{m,stg2}}{R_{in}}$. By assuming $R_{tot} = 500\Omega, Q = 10, R_{sw} = 20$, from Figure 3.10, β becomes equal to 0.18, which leads to $g_{mAUX} \approx 2 g_{m,stg2}$. For a typical choice for $g_{m,stg2}$ (e.g. 40 mS), g_{mAUX} should be as large as 80 mS, which can significantly reduce LNTA selectivity. As a result, in our design, g_{mAUX} was selected in such way to achieve only partial noise cancellation.

3.2.2 Inverter-Based Class-AB CS Stage

In Figure 3.21, the auxiliary path is a simple inverter-based CS stage with a bias tuned for class-AB operation. The reason behind this is to avoid the power-linearity tradeoffs of traditional class-A amplifiers and attain higher dynamic ranges. To bias the CS stage for class-AB operation, the MOSFETs should operate in the weak inversion region [yusaw]. In the weak inversion region, the relationship between the drain current versus the gate-source voltage is exponential, similar to bipolar transistors, and is given by (3.44) [39].

$$I_d = I_0 e^{V_{gs}/nV_T} \tag{3.44}$$

As demonstrated by [5], for a single NMOS transistor biased in the weak inversion, when a large out-of-band jammer is present at the input of the LNTA together with a small desired signal, the small-signal gain of the desired signal increases as the blocker power increases; hence gain expansion in the V-I transfer function. The expansion effect can be exploited to offset the gain compression due to other devices in the signal chain [5], which can greatly improve the

desensitization point of the whole RX RF front-end. For the proposed LNTA, the compression may arise from transistors M_7 or M_6 in Figure 3.21 or the downconversion passive current mixer following the LNTA. Besides, it will be discussed in section 0 that expansion in the gain followed by compression improves the large-signal IMD performance.

To demonstrate the class-AB operation when the devices are biased in the weak inversion, the normalized transconductance of the inverter-based LNTA, using PSS analysis, is plotted as a function of the input power for various values of the transistors V_{dsat} in Figure 3.22. For this simulation, the LNTA is terminated with a 10 Ω load impedance. The W/L of the transistors has been chosen large and in such a way that $(g_m / I_D)_{NMOS} = (g_m / I_D)_{PMOS}$. From Figure 3.22, it is seen that as the transistors operate closer to the weak inversion region, the gain expansion increases.

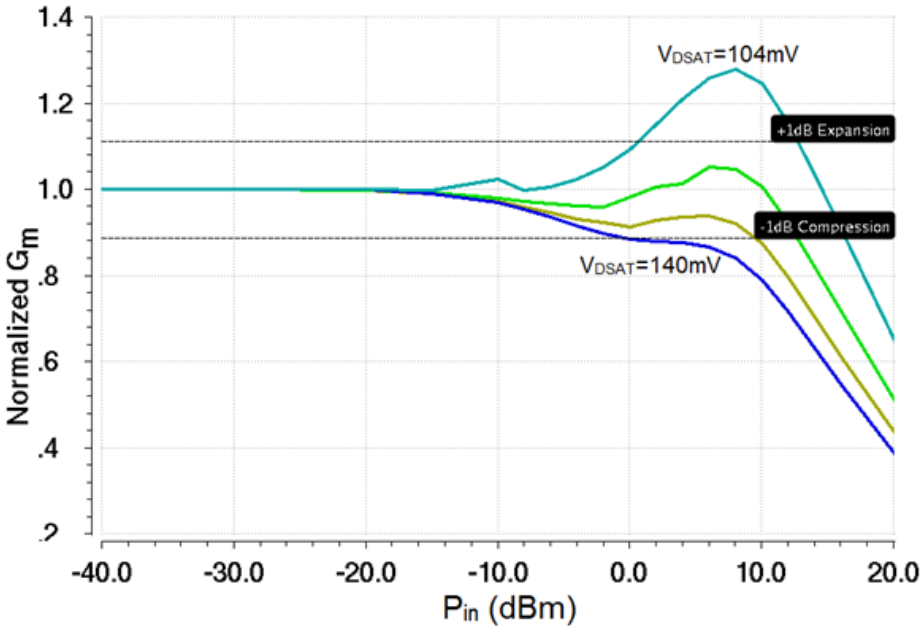


Figure 3.22: Simulated normalized transconductance of the push/pull CS stage as a function of input blocker power for various biasing conditions.

3.2.2.1 Large-Signal IMD Sweet Spot in Class-AB Operation*

It has been mathematically analyzed in [40] and intuitively explained by [31] that gain expansion in the AM/AM characteristic of an amplifier followed by gain compression, or vice-versa, leads to a large-signal IMD sweet spot, similar to the concept widely used in power amplifiers. This property is common in class-AB amplifiers [40].

To demonstrate the large-signal IMD sweet spot in class-AB amplifiers, the common-source stage simulated in the previous section is employed here. The intermodulation ratio (IMR) and the normalized g_m of the amplifier are simulated and plotted in Figure 3.23 for various g_m/I_D of the transistors, which corresponds to various operating regions (large g_m/I_D corresponds to sub-threshold region. As g_m/I_D reduces, devices enter into the saturation region). It can be seen that for $g_m/I_D = 13$ both small-signal and large-signal IMR measures are optimized.

Moreover, to show the importance of the load impedance on the class-AB operation of the amplifier, as discussed in section 3.1 for the common-gate push/pull stage, the bias point of the

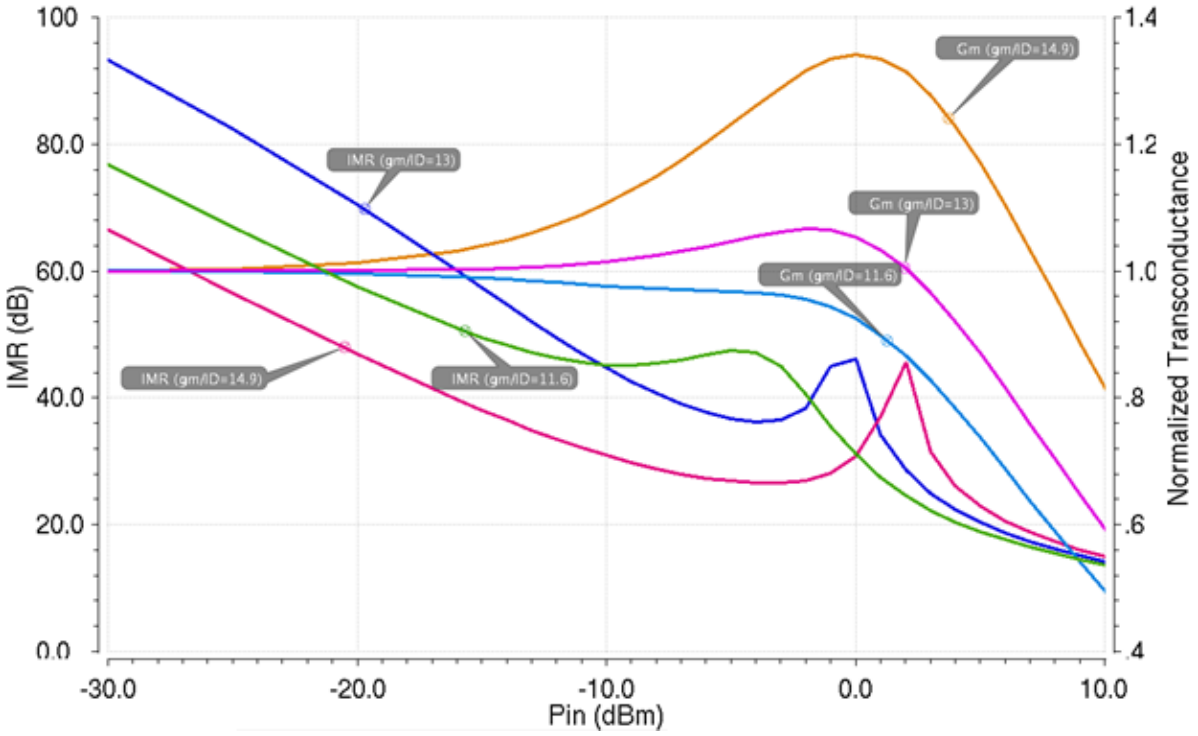


Figure 3.23: IMR and normalized g_m as a function input blocker power for various operating regions specified in terms of g_m/I_D.

transistors is fixed ($g_m/I_D = 13$ *or* $vdsat = 108mV$) and the load impedance is varied. The results are shown in Figure 3.24. It is seen that as the load impedance increases the amplifier starts to compress and both the small-signal and large-signal IMR measures are exacerbated.

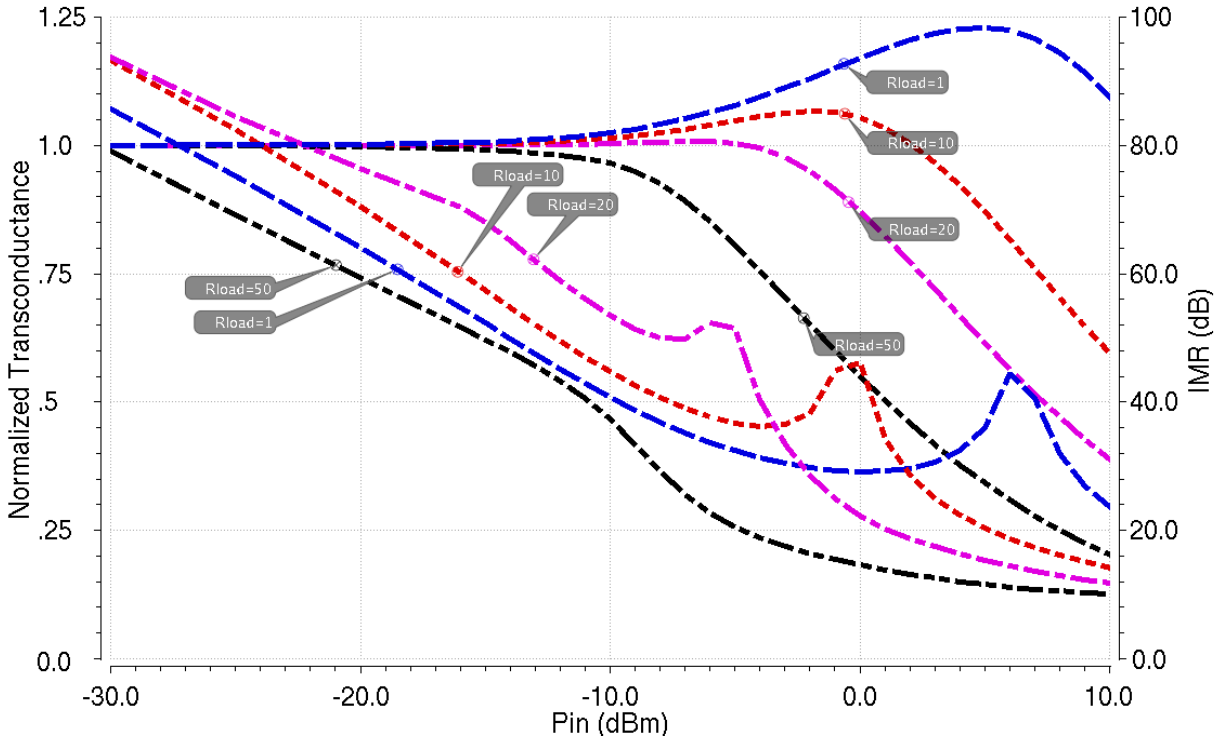


Figure 3.24: The impact of the load impedance on the push/pull class-AB common-source amplifier linearity and large-signal behavior.

3.3 Final Design and Simulation Results

Relying on the provided analysis and intuition, the proposed LNTA of Figure 3.21 was designed and implemented in 65-nm RF CMOS process with low-threshold devices and a supply voltage of 1.5 V. The details of the bias and the 25% duty-cycle cock generation circuitry are discussed in section 4.1, while in this section only the biasing conditions and circuit parameters are disclosed. For added accuracy, all the layout parasitics (including parasitic resistors and capacitors) and the bondwire inductance for all the external connections are taken into account for the simulations of this section.

The proposed LNTA of Figure 3.21 is repeated again in Figure 3.25 with all the circuit parameters annotated on the figure. It can be seen that the CS stage bias is tuned for class-AB operation (by choosing large g_m/I_D for M_7 and M_8), and $vdsat \approx 220mV$ for M_6/M_5 to obtain a

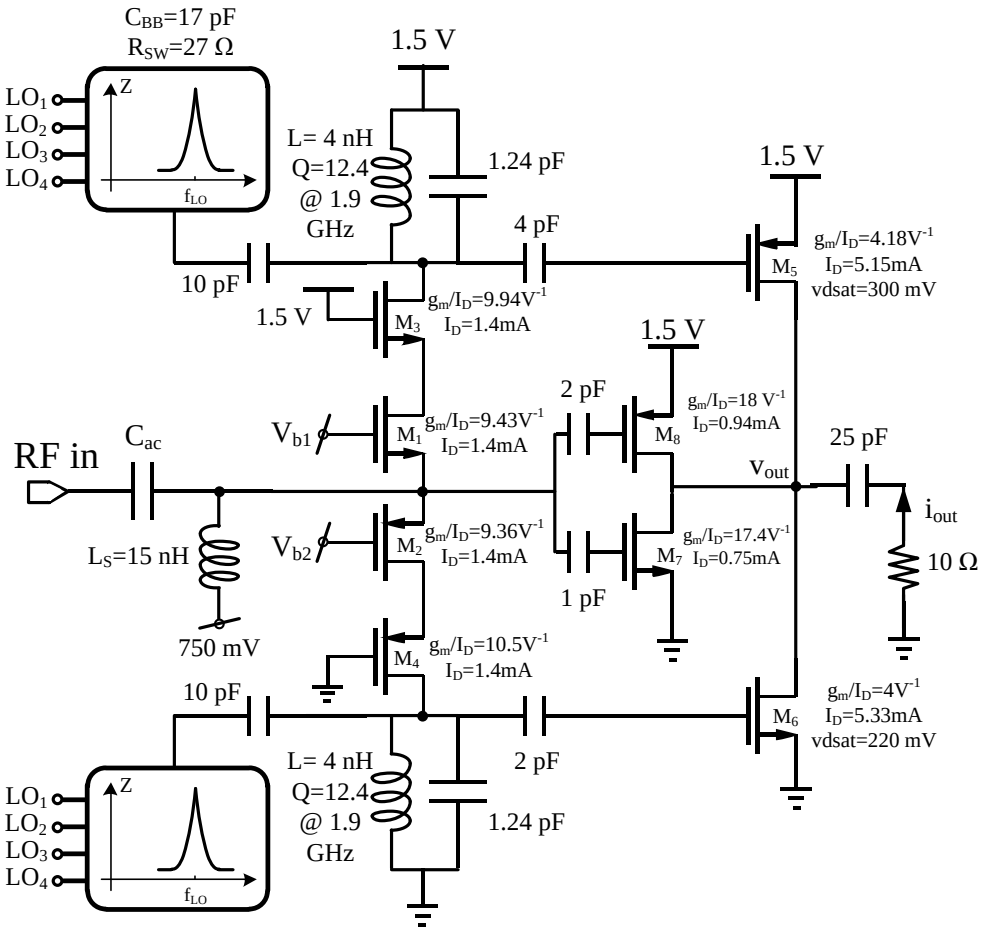


Figure 3.25: Final design of the proposed LNTA with annotated circuit parameters.

good V-I linearity [37].

To characterize the load impedance at the output of the CG stage, we performed hand analysis to find R_{tot} and C_{tot} (as explained in 3.1.2) assuming $g_m r_o \approx 5.7$ and $r_o \approx 450\Omega$ for M_1 to M_4, based on DC simulations. From the calculations we found $R_{tot} \approx 456\Omega$, $\omega_{tank} \approx 1.9GHz$, and $Q \approx 9.8$. Based on Figure 3.10 , for this value of Q-factor, $R_{in-band}$ becomes a strong function of R_{sw}. This suggests R_{sw} should be made large to achieve low NF.

However, for best linearity, it is desirable to make R_{sw} as small as possible to minimize the out-of-band load impedance of the CG stage. Thus, we made a compromise between NF and linearity by choosing $R_{sw} \approx 27\Omega (W/L = 40\mu/60n)$. $R_{in-band}$ now becomes equal to $\approx 133\Omega$ using (3.12) and $\approx 181\Omega$ from the simulations. The discrepancy between these due values arises from non-zero rise/fall time (T_r / T_f) of the clocks. It should be emphasized that for the analysis of the HQBPF in section 0 it was assumed that the 25% duty-cycle clocks are perfectly square-wave. Obviously, this is not the case for real clocks. To investigate the effect of T_r / T_f, an ideal clock generator was employed with controllable T_r / T_f in the simulations, and $R_{in-band}$ versus T_r / T_f

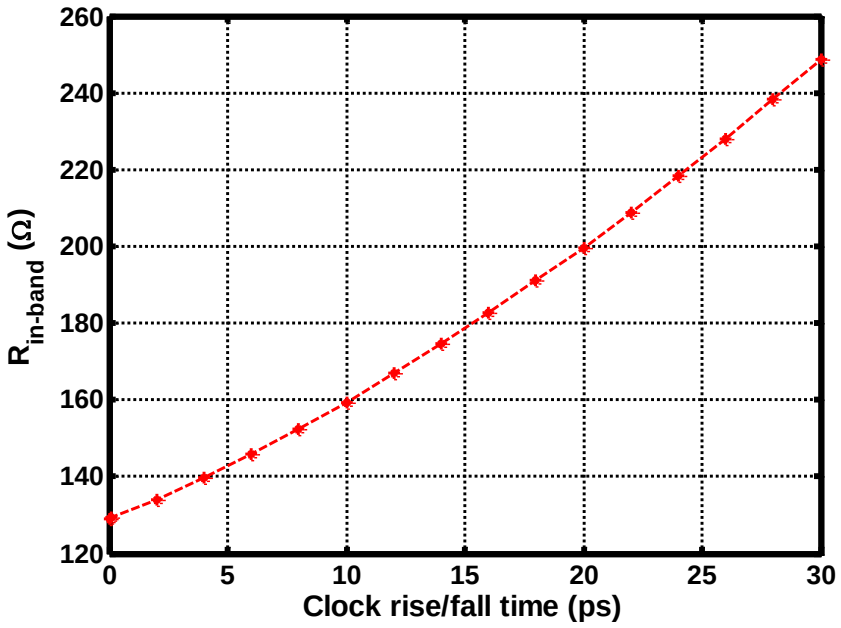


Figure 3.26: The effect of clock rise/fall time on the input impedance of the HQBPF.

was simulated. The results are shown in Figure 3.26. It can be seen that for small rise/fall times $R_{in-band}$ agrees well with the predicted value of 133Ω, and as T_r / T_f increases, $R_{in-band}$ becomes larger. This can be due to the fact that as T_r / T_f increases, the higher harmonics of LO[7], thus, the loss due to harmonic reupconversion reduces, which leads to higher $R_{in-band}$.

3.3.1 Gain, Selectivity, and S_{11} Simulations

Using PSS+PAC simulations in Spectre RF, the voltage gain of the LNTA for two cases when HQBPFs are enabled (tuned to the center frequency of 1.8 GHz), and when they are disabled is shown in Figure 3.27. When HQBPFs are enabled, the 3-dB RF bandwidth is equal to 25 MHz and we can achieve around 9 dB rejection at the frequency offset of 100 MHz. The LNTA transconductance, defined as $g_{mLNTA} = i_{out} / 2v_{source}$, is also plotted in Figure 3.28. Nevertheless, it should be noted that in the analysis of section 3.1.1, it was assumed that the resonance frequency of the LC tank (ω_{tank}) is equal to ω_{LO}. From the simulations, we concluded that $\omega_{tank} = \omega_{LO}$ leads to maximum in-band gain and symmetry around ω_{LO}. As ω_{tank} deviates from ω_{LO}, the out-of-band impedances in the upper-sideband and lower-sideband are no longer equal to R_{sw}. To avoid

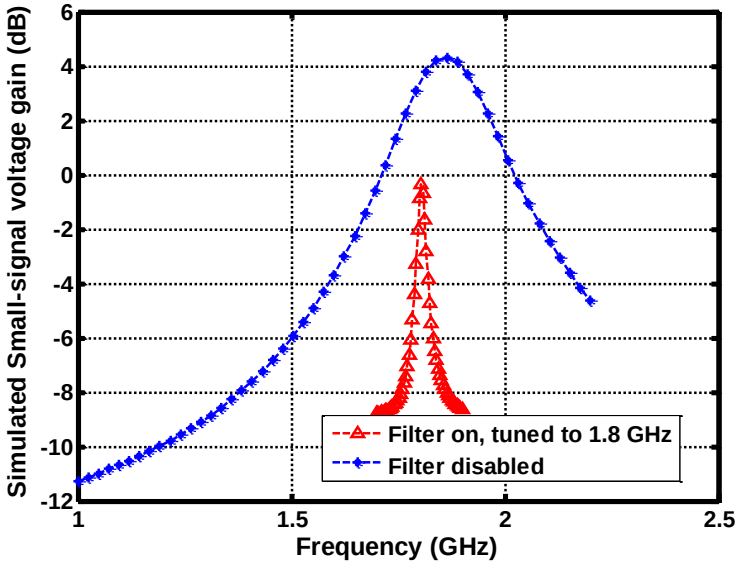


Figure 3.27: Simulated small-signal voltage gain (R_L=10 Ω).

[7] High-order harmonic contents of a trapezoid-waveform-like LO are lower than a square-wave LO due to slower transitions. [http://www.westbay.ndirect.co.uk/periodic.htm/]

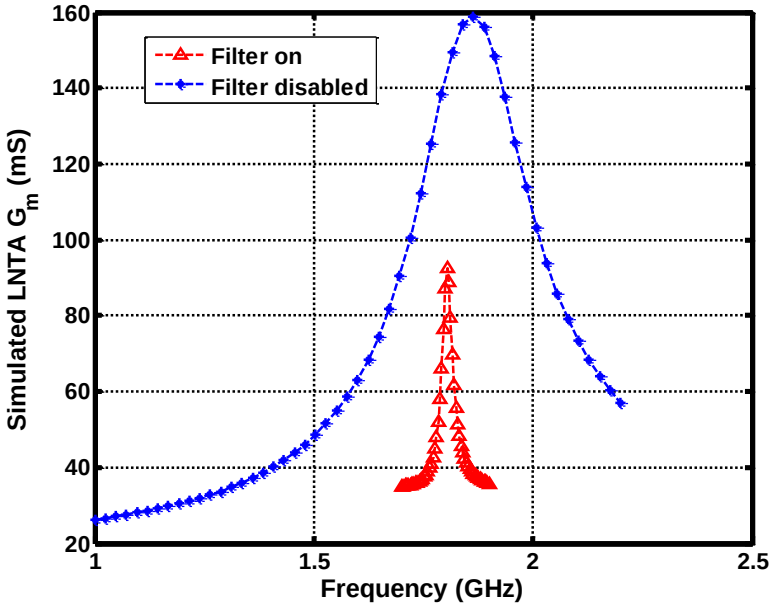


Figure 3.28: Simulated LNTA transconductance.

this issue and to enable wideband operation of the LNTA, a capacitor tank should be used to tune ω_{tank} to the desired LO frequency. In this work, due to shortage of time, the LNTA was only designed and implemented for the tuned center frequency of 1.85 GHz.

To show the wideband 50-Ω matching property of the LNTA, the S_{11} as a function of frequency is plotted in Figure 3.29.

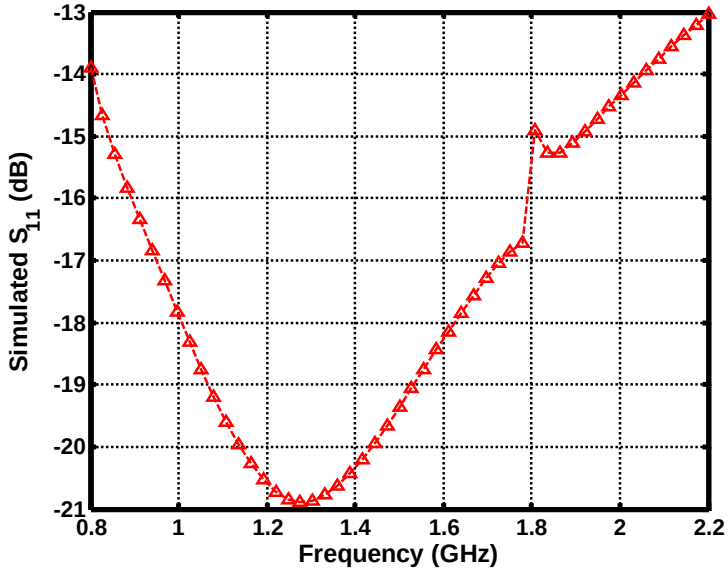


Figure 3.29: Simulated S_{11} for the LNTA tuned to 1.8 GHz (including the input bondwire and L_s).

3.3.2 Noise Simulations

The simulated in-band NF of the LNTA is 4.9 dB with HQBPFs enabled and tuned to the center frequency of 1.8 GHz, using PSS+PNOISE simulations. By disabling the filters, the in-band gain increases, hence the NF reduces to 4.4 dB. At the presence of no blocker, the LNTA can operate in this mode to achieve 0.5 dB better NF performance. However, the NF increase penalty when the filters are on is much lower compared to [6], in which the NF degrades by around 5 dB (NF=3.1 dB without HQBPFs, NF≈8 dB with HQBPFs).

In addition, when the CS stage was disabled, the simulated in-band NF of the LNTA became equal to 7 dB, which shows the effectiveness of using the auxiliary CS path to improve the NF.

According to Figure 3.30, the LNTA center frequency (where the minimum NF and maximum gain are achieved) has shifted by around 5 MHz with HQBPFs on and tuned to 1.8 GHz. The reason is the difference between the resonance frequency of the LC tank and ω_{LO}, which can be alleviated by incorporating a capacitor tank to fine-tune the LC tank resonance frequency.

To see how the LNTA operates at the presence of a large blocker, PNOISE analysis was performed while sweeping the amplitude of a CW input blocker at 100 MHz frequency offset, with the HQBPFs enabled and tuned to 1.8 GHz. The result is plotted in Figure 3.31.

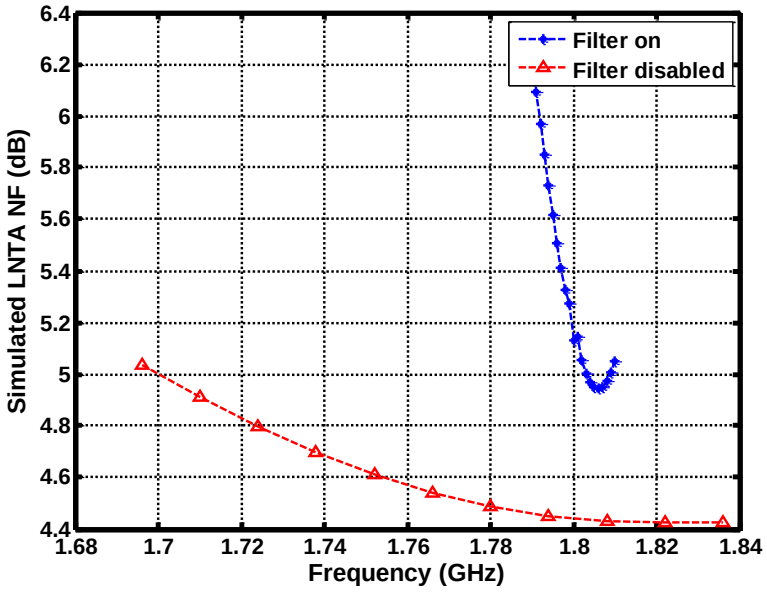


Figure 3.30: Simulated LNTA NF.

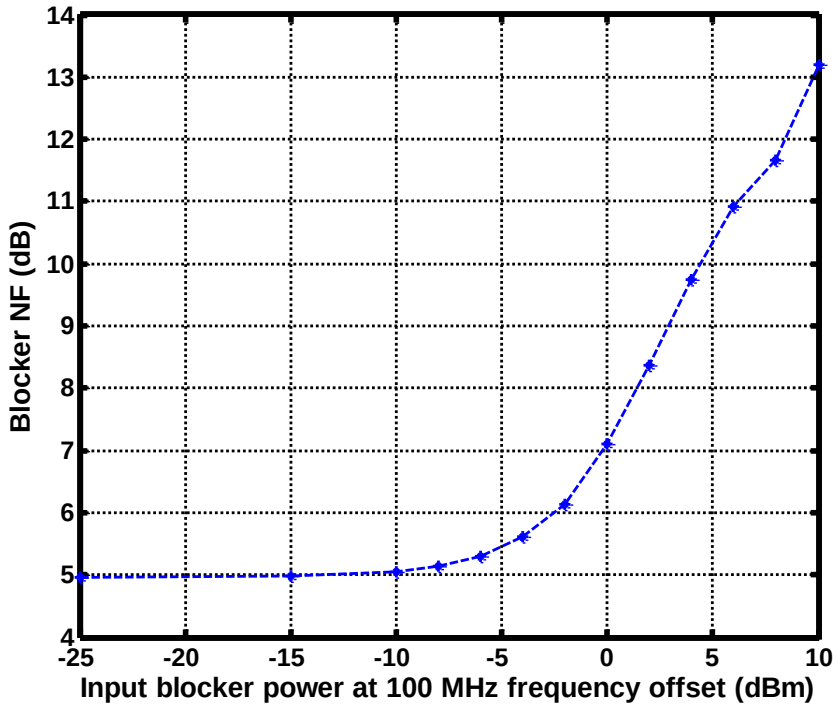


Figure 3.31: Simulated blocker NF for a blocker at 100 MHz frequency offset (LNTA tuned to 1.8 GHz).

3.3.3 Desensitization Simulations

The small-signal transconductance of the LNTA, tuned to 1.8 GHz, is determined by applying a CW blocker at 100 MHz frequency offset and a small desired in-band CW signal, using a PSS+PAC simulation. Figure 3.32 shows the change in the small-signal g_m of the LNTA as a function of input blocker power. It can be seen that -1-dB desensitization point of +7.5 dBm is attained, which is a very competitive number for such value of NF (4.9 dB) for the LNTA. In addition, the HQBPFs are disabled to demonstrate the effectiveness of the HQBPFs in achieving improved large-signal performance. It is seen that when the HQBPFs are disabled the -1-dB desensitization point reduces to -10 dBm.

Due to class-AB operation of the CS auxiliary path and the expansion in the input impedance of the HQBPFs, explained in section 3.1.4, we can see a relatively large gain expansion followed by compression in plot of Figure 3.32. Although the gain expansion exceeds the +1 dB point for +4 dBm input blocker power, it can be expected that this gain expansion will be compensated with the gain compression of the downconversion mixer following the LNTA.

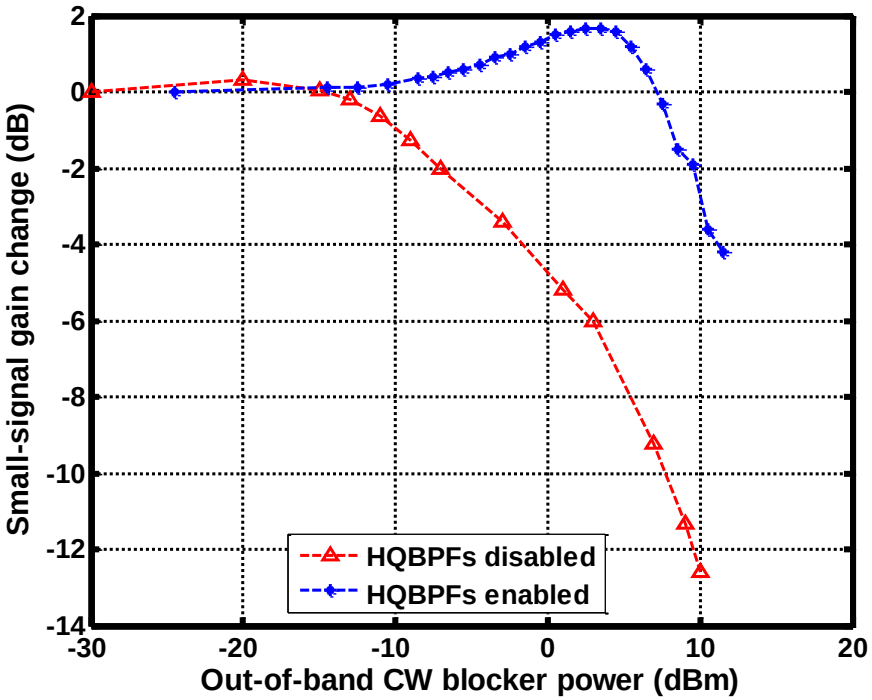


Figure 3.32: Simulated small-signal gain change versus the input power of a CW blocker at 100 MHz frequency offset.

3.3.4 Intermodulation Simulations

The simulated in-band IIP3, using QPSS analysis, is around +13 dBm at tuned center frequency of 1.8 GHz. This relatively large value of IIP3 was expected due to the complementary PMOS/NMOS structure of the LNTA.

To simulate out-of-band IIP3 and confirm the IMD cancellation due to the expansion/compression of the gain for large out-of-band blockers (shown in Figure 3.32), two CW blockers with equal powers at 1.9 GHz and 2 GHz were applied to the LNTA, and the in-band IMD product at 1.8 GHz at the output was recorded. The IMD product was then referred to the input by using the small-signal in-band gain simulated in section 3.3.1 and plotted as a function of the input blocker power, as shown in Figure 3.33. It is seen that the notch in the IMD curve occurs around +2 dBm blocker power, which corresponds to the large-signal IMD sweet spot [40] discussed in section 0. To find the linearity performance in terms of the conventional IIP3 metric, (3.45) is used to extrapolate IIP3 for each point [24].

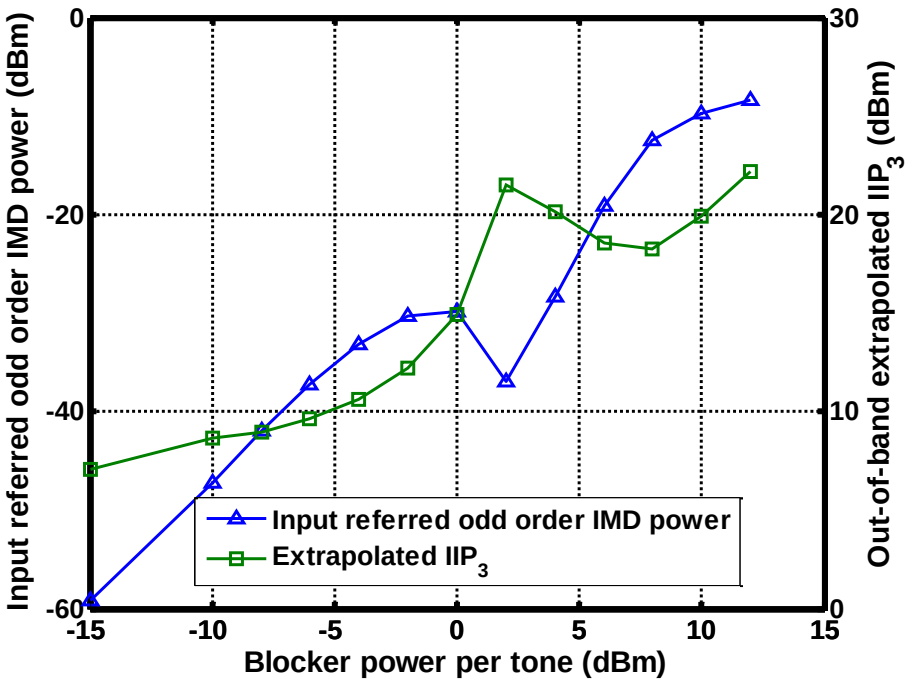


Figure 3.33: Simulated input referred odd order IMD power and extrapolated out-of-band IIP3.

$$IIP3 = P_{in} + \frac{P_{in} - IMD3_{in,referred}}{2} \tag{3.45}$$

[35]

Chapter 4

TEST CHIP AND MEASUREMENT RESULTS

4.1 Test Chip Implementation Issues

A test chip has been fabricated in this project in 65-nm RF CMOS process using low-threshold voltage devices. The schematic of the implemented circuit on this test chip is shown in Figure 4.1. The test chip includes the proposed LNTA together with the 25% clock generation circuitry, the LNTA termination impedance, which emulates the input impedance of downconversion

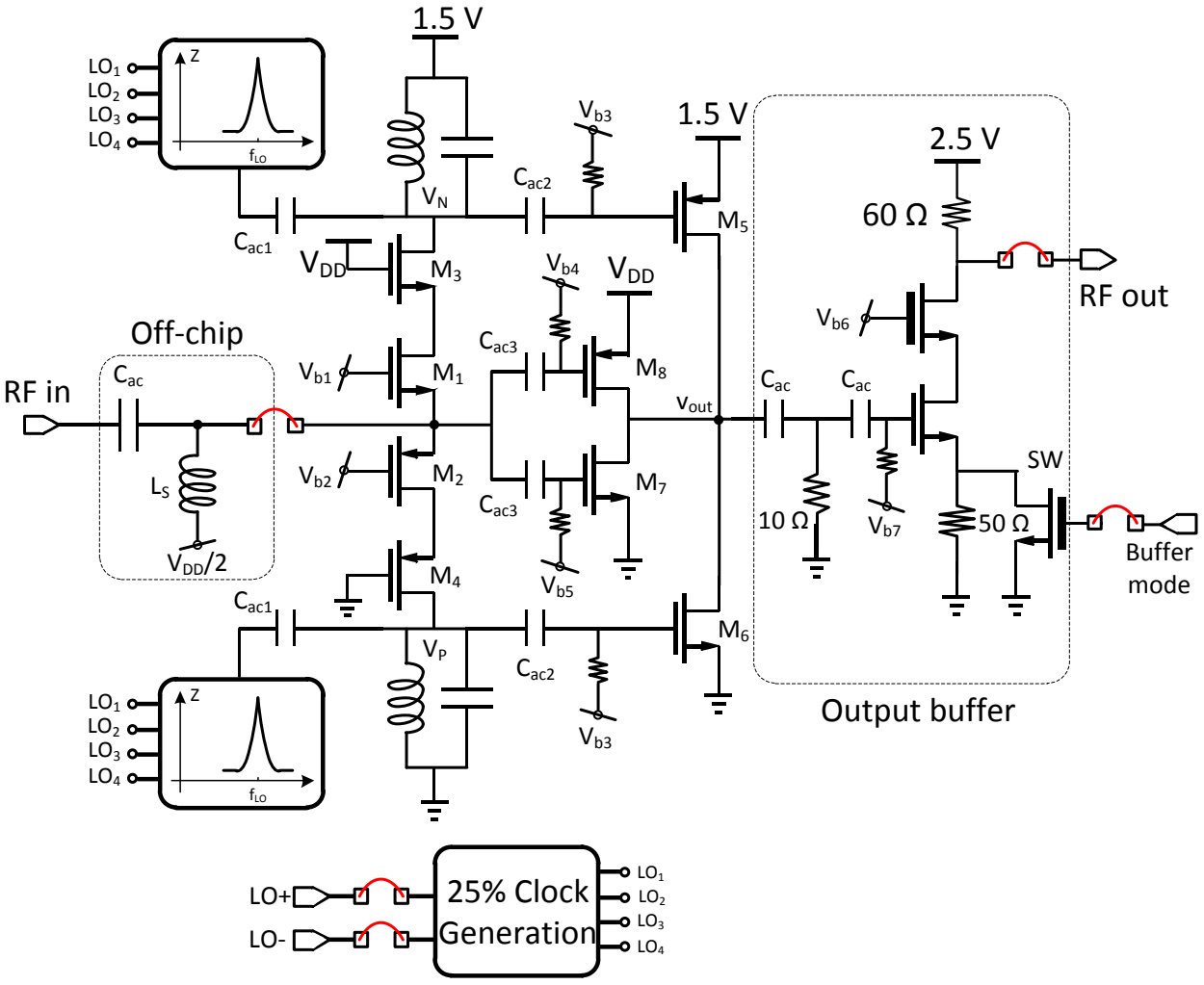


Figure 4.1: The schematic of the implemented circuit on the test chip.

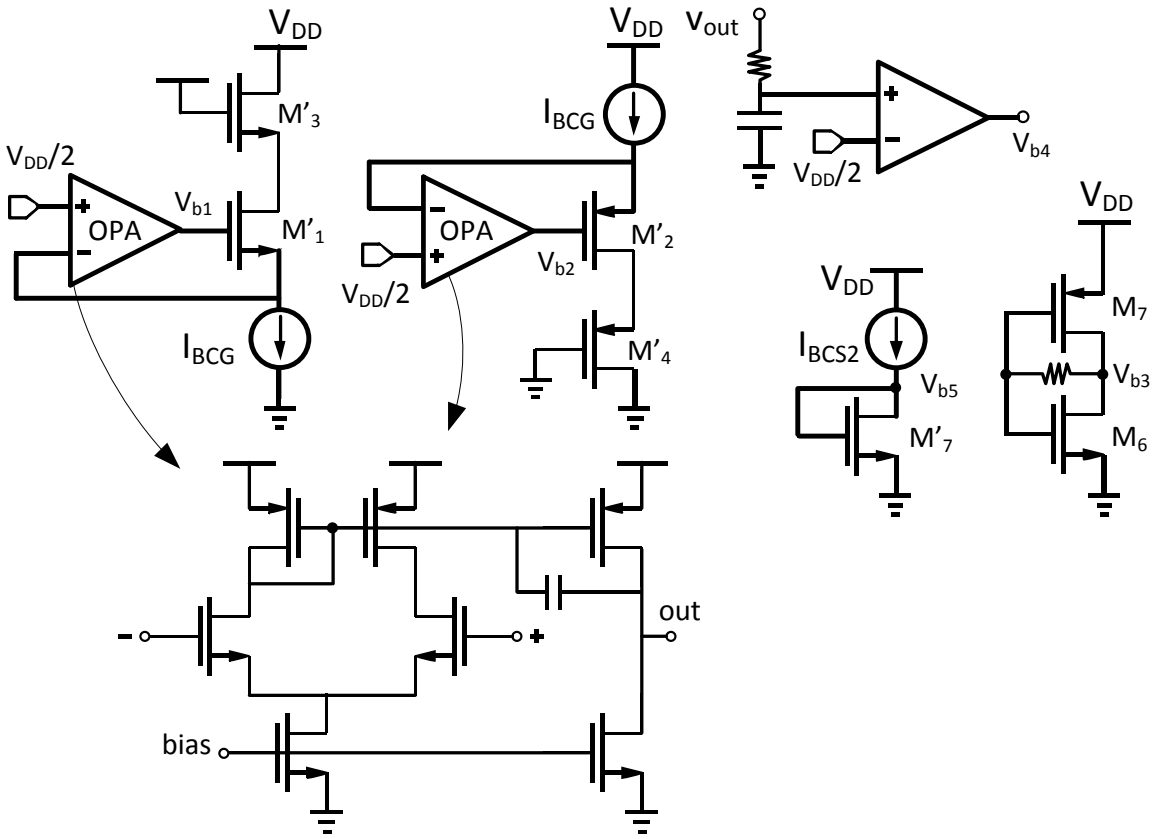


Figure 4.2: The simplified schematic of the bias generation circuitry.

passive current mixer that follows the LNTA, and an output buffer. The simplified schematic of bias generation circuitry is shown in Figure 4.2. For the common-gate input stage, a replica biasing scheme with feedback is used to fix the source voltage at $V_{DD}/2$ and ensure the desired bias current. This chapter discusses some issues regarding the circuit and layout implementations.

4.1.1 LNTA Termination

Since the proposed LNTA is used in the context of current-mode passive mixer receiver architecture, it is supposed to drive a current passive downconversion mixer with relatively small input impedances. Therefore, to emulate the actual loading conditions, the LNTA was terminated with an on-chip passive 10 Ω resistor. The on-chip resistor was preferred over the approach used in [29], which employs a transimpedance amplifier (on-chip resistive feedback amplifier) to produce the desired load impedance for the LNTA. Since the output current swing of LNTA under blocking conditions is large and the value of the load impedance is relatively small, using an on-chip passive 10 Ω resistor was preferred over other methods, which normally use active

elements (transistors) that can adversely affect the linearity of the circuit and corrupt the measured data. In addition, due to practical reasons it is not possible to directly measure the transconductance of the LNTA, and it is necessary to convert back the LNTA output current to voltage. This task is simply done by the 10 Ω output load impedance. The absolute value of the resistor is of important since it determines the voltage gain and the linearity of the LNTA.

One disadvantage of on-chip passive components is that their absolute value is prone to relatively large process variation, although by proper layout their relative matching value can be very accurate. In order to minimize the effect of process variation, poly resistors without salicide (*rppolywo_rf*) were used. Compared to salicided poly resistors, *rppolywo_rf* has higher resistance for the same dimensions, so they occupy more area on chip if they are used to implement low resistance values. But in this test chip, this was a trivial issue. For the best absolute accuracy, 70 unit cells of *rppolywo_rf* with $W = L = 2\,\mu m$ ($R_{unit} = 707.8\,\Omega$) were used, which according to the simulations leads to about ±13% variations over the corners.

To further reduce the errors due to process variation of the resistors, a dummy 10 Ω resistor was implemented in parallel with the main resistor; consequently, by measuring the of value the dummy resistor via a dedicated pin, the absolute value of the LNTA gain can be corrected. As shown in Figure 4.3, the unit cells of the dummy and the main resistors were interleaved and placed adjacent to each other, so that the dummy resistor would accurately follow the mismatches in value of the main resistor.

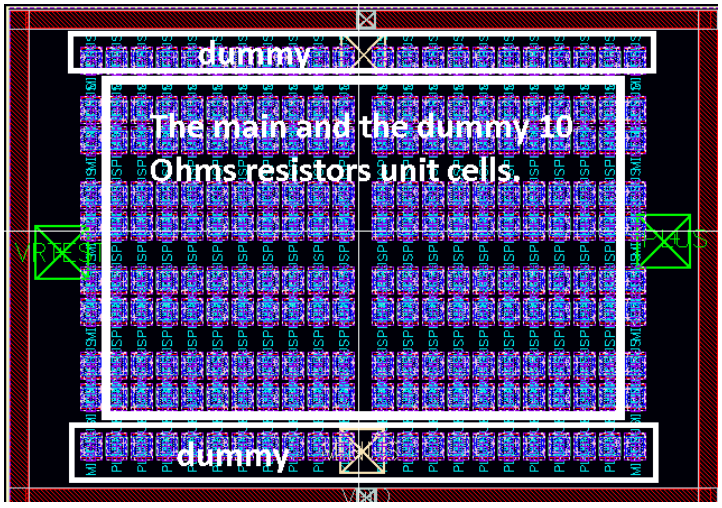


Figure 4.3: The layout of the main and dummy 10 Ω resistors including the protection dummy resistor ring.

4.1.2 Output Buffer

The available measurement instruments are typically designed for 50 Ω impedance matching (as are the cables). So connecting the output of the LNTA directly to the measurement instrument will disturb the load impedance at this node and render the measurements rather inaccurate. Moreover, the bondwire and the PCB traces parasitics will also affect the loading conditions of the LNTA. To avoid this issue and for more accurate NF measurements, it was necessary to employ an output buffer capable of driving 50 Ω impedance. The schematic of the output buffer, which is a simple common-source amplifier with resistive load, is illustrated in Figure 4.4.

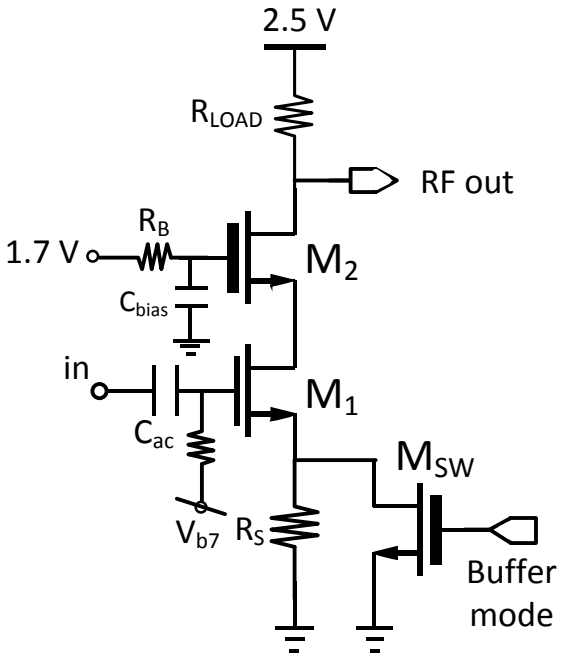


Figure 4.4: Output buffer with high/low gain modes.

The output buffer can operate in two modes, namely, high gain and low gain modes by using a 2.5 V thick-oxide switch scheme. As will be discussed in section (4.2), for noise measurements a NF analyzer (Agilent N8972A NFA) was deployed. Although NFA can measure the NF more accurately compared to other methods[8], its accuracy is a function of DUT gain. Because of the relatively small load impedance of the LNTA (10 Ω), the simulated in-band voltage gain is about 7 dB, which can render the measurements very inaccurate. For noise and s-parameter

[8] http://www.maximintegrated.com/app-notes/index.mvp/id/2875

measurements, the buffer was set to the high-gain mode by bypassing the degeneration resistor R_s and using relatively high DC current levels (20 mA) for M_1 and M_2 to maximize the buffer gain. For sufficient voltage headroom for the cascode transistor M_2, a high supply voltage of 2.5 V was used, and to avoid oxide breakdown, thick-oxide device were used for M_2.

Due to the silicon area limitations, the output buffer was not fabricated and characterized separately, and we relied on the simulations to de-embed its effects. Since it is rather difficult to de-embed the effect of the output buffer on the LNT linearity measurements such as IIP_3 and desensitization point (B_{-1dB}), we had to ensure that the output buffer linearity performance would not be a limiting factor. This was achieved by degenerating M_1 (hence low-gain mode) with a 50 Ω resistor (R_S). Table 4.1 summarizes the simulated performance of the output buffer for the two operating modes after extraction of the layout parasitics. Figure 4.5 demonstrates the gain and the input-referred noise versus the frequency for the desired operating range. From this figure, it can be seen that for the intended frequency range, the gain and the noise of the buffer remains rather constant.

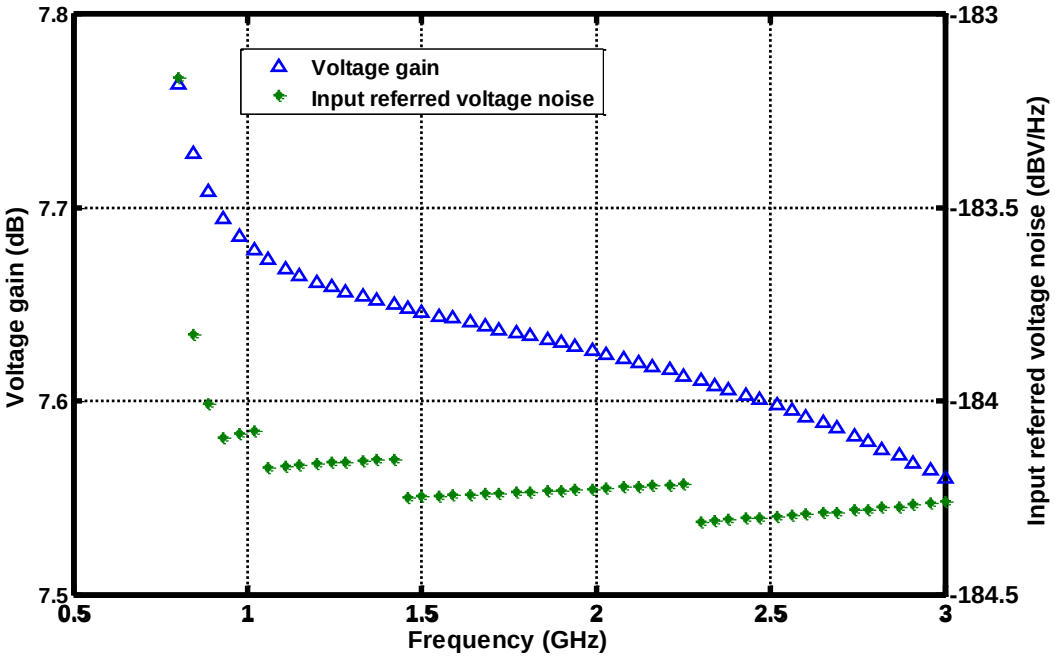


Figure 4.5: The simulated gain and input referred voltage noise of the buffer stage.

To be able to measure the large desensitization point of the LNTA, we had to make sure that the LNTA output voltage swing caused by the blocker does not exceed the buffer compression point. Figure 4.6 shows the simulation results of the small signal gain change versus the blocker power at the output node of the LNTA as well as at the output of the buffer in low-gain mode. It can be inferred from this figure that for the intended value of B_{-1dB}, the compression of the output buffer does not have significant effect, and it only reduces B_{-1dB} by 1 dB.

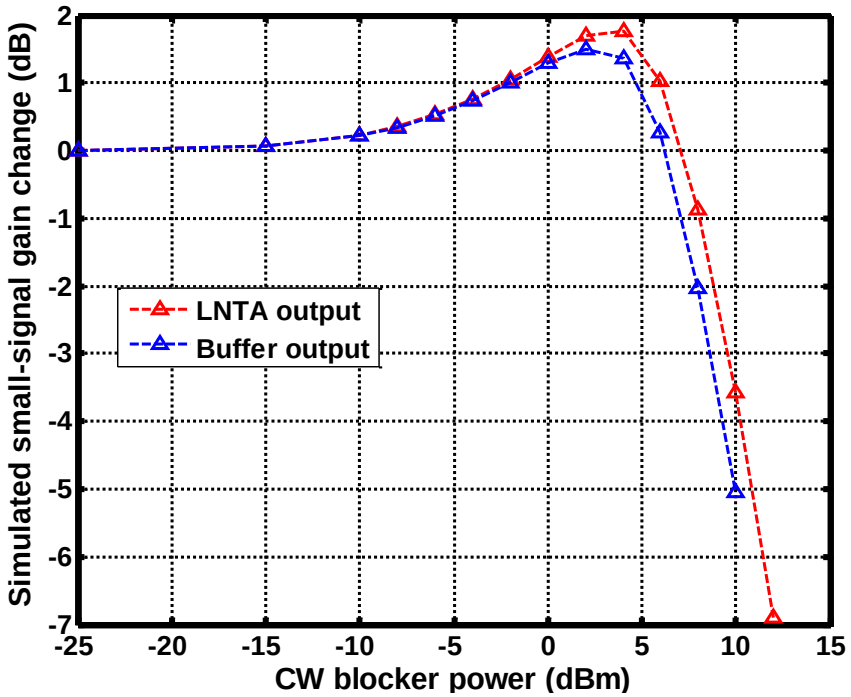


Figure 4.6: Simulated small-signal gain change vs. blocker at the output of the LNTA and the buffer stage (the output buffer is set to low-gain mode for best linearity performance).

To de-embed the noise contribution of the 10 Ω load impedance and the buffer stage, the simplified schematic of Figure 4.7 was used to find the relationship between the NF of the LNTA (NF_{LNTA}) and the measured NF (NF_{meas}), which is given by (assuming $R_{oLNTA} \gg R_1$):

Mode of operation	I_{bias} (mA)	Gain (dB)	Input referred voltage noise (dBV/Hz)	Input compression point (mV peak)	IIP_3 (dBm)	S_{22} (dB)
High-gain	20.6	7.6	-184.2	241	8.1	-20
Low-gain	8.6	-7.5	--	541	17	-26

Table 4.1: Summary of output buffer simulated performance including the layout parasitics and the bondwire effect.

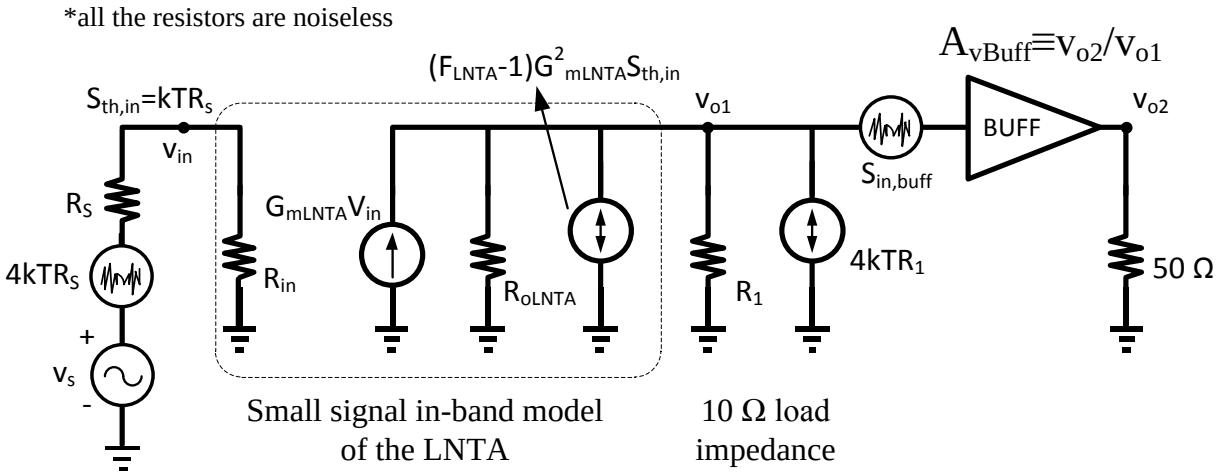


Figure 4.7: Simplified schematic of the LNTA and the buffer stage including all the noise sources for NF calculations.

$$F_{meas} \approx F_{LNTA} + \frac{4R_1}{R_s} \cdot \frac{1}{(A_{vLNTA})^2} + \frac{S_{in,buff}}{(A_{vLNTA})^2 S_{th,in}} \tag{4.1}$$

where F_{LNTA} is the noise factor of the LNTA, R_1 is the 10 Ω load impedance, R_s is the source impedance, which is 50 Ω, $S_{th,in}$ is the single-sided voltage noise PSD at the input of the LNTA due to R_s thermal noise, and $S_{in,buff}$ is the single-sided input-referred voltage noise PSD of the buffer stage assuming a noiseless 10 Ω and 50 Ω termination at its output and output, respectively. The voltage gain of the LNTA in denoted as A_{vLNTA} and is given by:

$$A_{vLNTA} \equiv \frac{v_{o1}}{v_{in}} \approx G_{mLNTA} \times R_1 \tag{4.2}$$

where G_{mLNTA} is the effective in-band transconductance of the LNTA. By finding A_{vBuff} and $S_{in,buff}$ through simulations and measuring $A_{vLNTA} \times A_{vBuff}$ and F_{meas}, the noise figure of the LNTA can be calculated through (4.1) with a good approximation.

4.1.3 25% Clock Generation

To generate the 25% duty-cycle clocks an on-chip divide-by-two, which is driven by $2\times f_{LO}$, provides quadrature 50% duty-cycle clocks at the desired LO frequency, as shown in Figure 4.8. By using four NAND gates (Figure 4.9) the 50% duty-cycle clocks are then used to generate 25% quadrature clocks [6].

The 25% clock generation circuitry consumes 15.5 mA at 1.2 supply voltage.

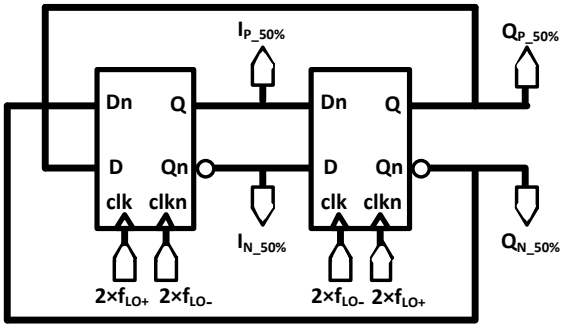


Figure 4.8: Divide-by-two simplified schematic [41].

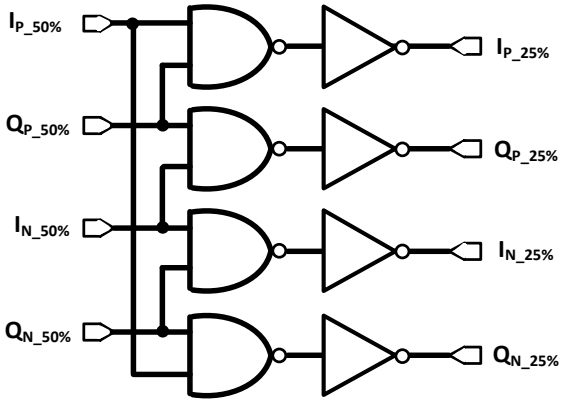


Figure 4.9: 25% duty-cycle clock generation using 4 NAND-gates [6].

4.2 Experimental Setup

The test chip was implemented in TSMC 65nm RF CMOS process and its die microphotograph is shown in Figure 4.10. To avoid package parasitic, the test chip was directly bondwired to the PCB, which is shown in Figure 4.11.

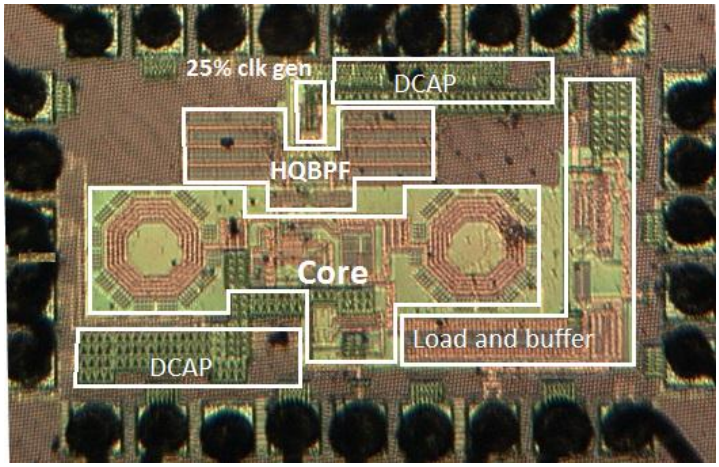


Figure 4.10: Die microphotograph.

As explained earlier, in section 0, to improve the impedance matching of the input stage and to maintain the proper input common-mode voltage of the LNTA, a 15 nH external inductor was used. To avoid PCB trace parasitics, a low profile 0402 SMD package inductor was chosen and placed very close to the input pin of the LNTA, as shown in Figure 4.12. To compensate for the

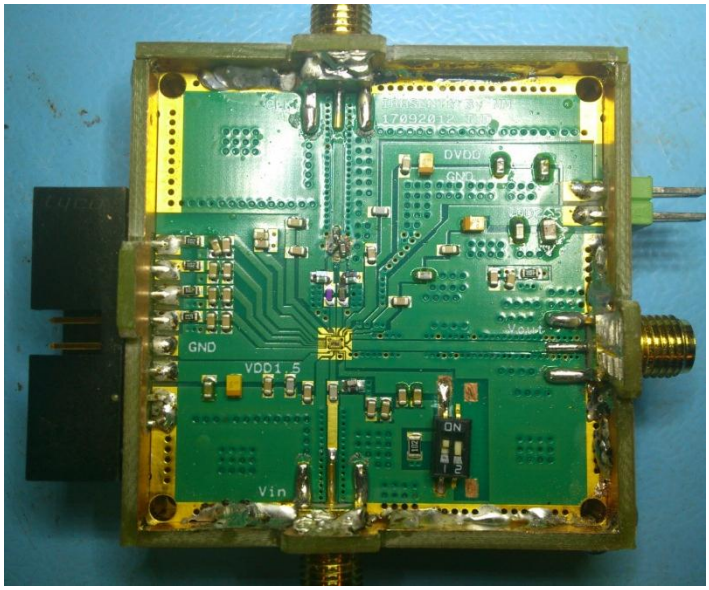


Figure 4.11: Experimental implementation of the proposed LNTA.

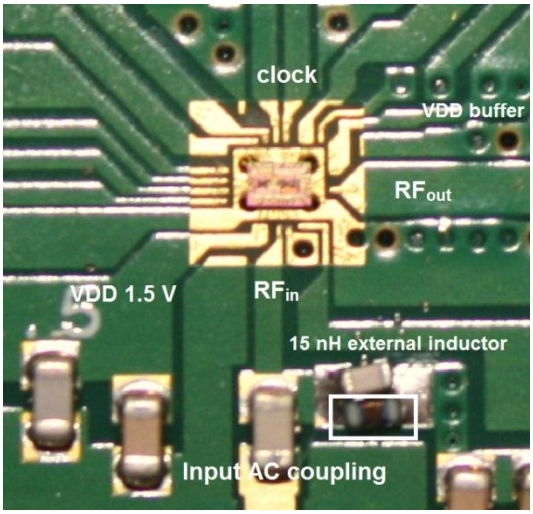


Figure 4.12: Zoomed-in view showing the bondwired test chip and the input 15 nH inductor.

effect of the bondwire parasitic inductance, an external capacitor parallel to the 15 nH inductor was also employed and its value was calculated from simulations assuming a typical value of 1 nH inductance for a bondwire.

A picture of the experimental setup is shown in Figure 4.13, and the setup schematic for s-parameter measurement, NF measurement, and desensitization point and IMD measurements are shown in Figure 4.14. The 2×LO signal was generated externally by the Agilent E4438C Vector Signal Generator for low phase-noise performance, and it was applied to the differential pins of the test chip via the Johanson 3600BL14M050 balun.

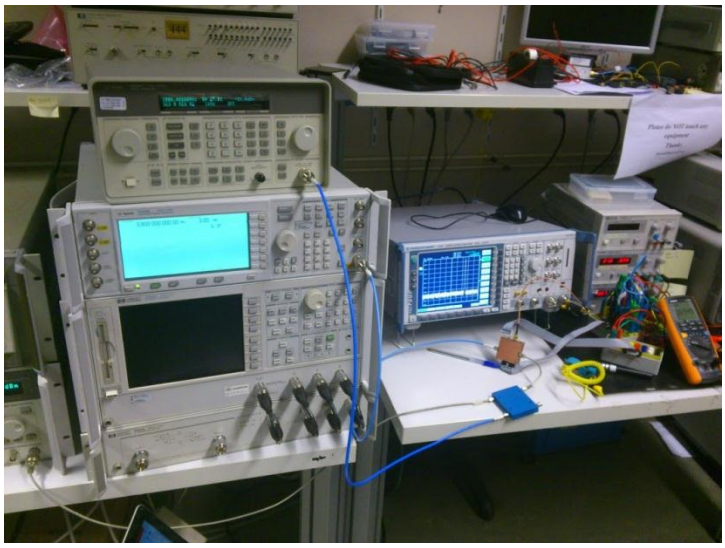


Figure 4.13: Picture of the experimental test setup.

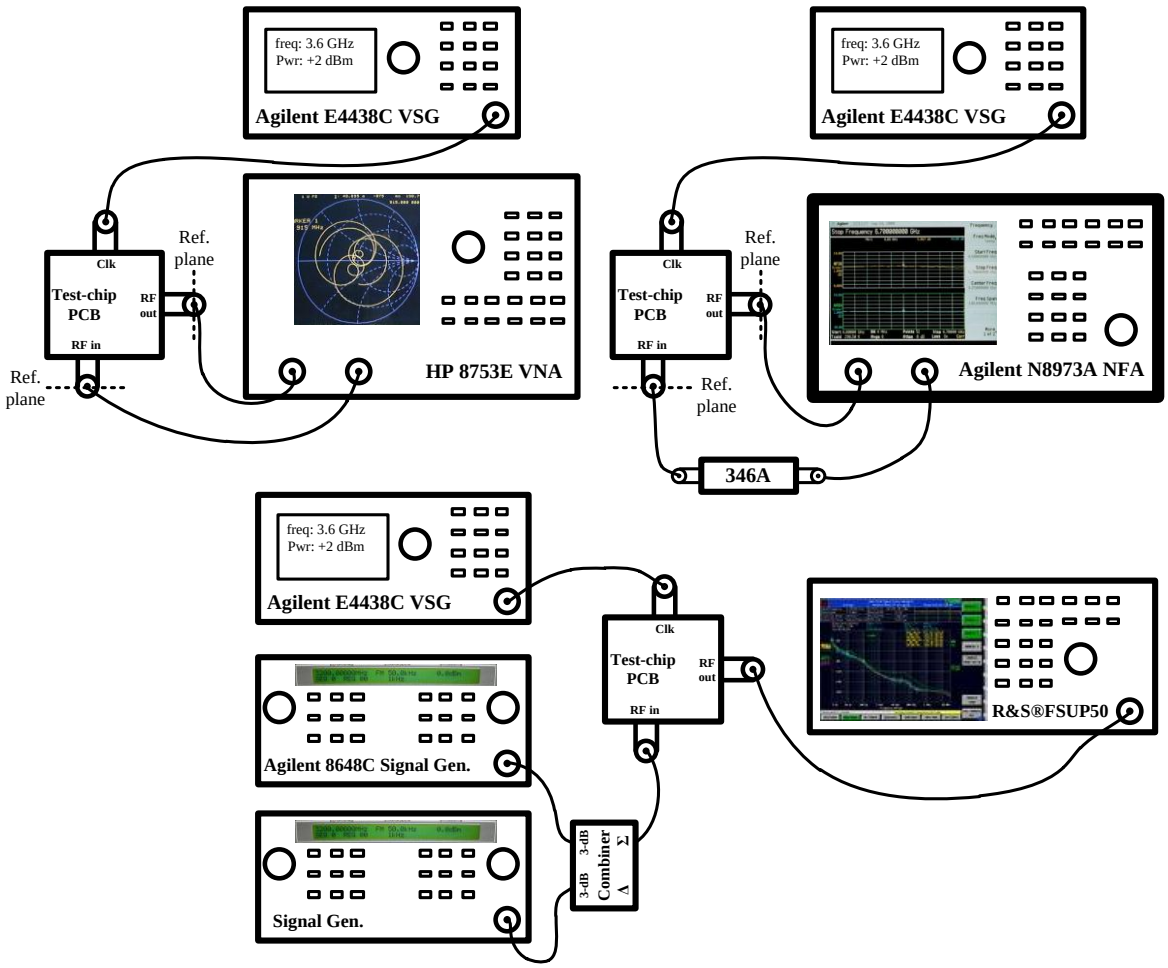


Figure 4.14: Setup schematics for various measurements

The S-parameters were measured using HP 8753E vector network analyzer (VNA). The VNA was calibrated using the full 2-port short-open-load-thru (SOLT) calibration method to de-embed the effect of the cables and connectors up to the SMA input on the test board. For noise figure measurements, the Agilent N8973A NF analyzer (NFA) together with 346A noise source was used. Due to imperfections in the HQBPFs, a relatively small LO leakage (with approximately -55 dBm power) was measured at the output, which could saturate the input of the NFA. To prevent that, the sweep range of the input frequency of the NFA had to be chosen carefully. For desensitization and IMD measurements, two signal generators were exploited, and their power was added together with a 3-way power divider. To de-embed the cable and power divider loss, the output power of the power divider was measured and recorded by R&S®FSUP50 signal source analyzer with a reference power level for the signal generators. This way we could accurately measure the actual power level at the SMA input of the PCB board.

4.3 Measurement Results

4.3.1 Small-Signal Measurement Results

Figure 4.15 shows the normalized gain of the test chip for different clock frequencies measured by the vector network analyzer. It should be emphasized here that the measured S_{21} also includes the gain of the buffer stage. Therefore, the LNTA transconductance is plotted in Figure 4.16 after de-embedding the effect of buffer stage and LNTA load impedance.

Although the LNTA was designed for 1.85 GHz, from Figure 4.15 we can see that the center frequency has shifted to around 1.8 GHz in the measurements. This is explained by the fact that the resonance freuency of the LC tank is very sensitive to C_{tank} and for a parsitic capacitance of 100 fF, the resonace frequency can shift by 50 MHz. The extra parasitic capacitance may arise from the layout traces.

According to Figure 4.15, the LNTA maintains relatively good selectivity of 6 dB between 1.5 to 2 GHz. As discussed in 3.3, it is possible to further improve the range of the operating frequency by employing a capacitor tank (which, due to lack of time, was not done for this test chip). Figure 4.15 also shows the gain when the HQBPF is disabled, which indicates no selectivity (or to be more accurate selectivity with relatively low-Q due to the LC tank). When there is no blocker present at the input of receiver, the on-chip high-Q bandpass filter can be turned off to

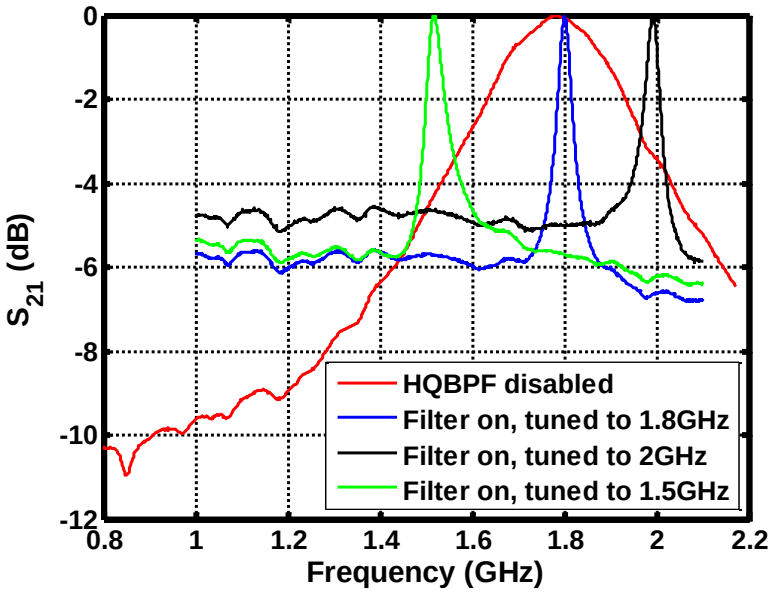


Figure 4.15: Measured normalized gain for various LO frequencies and with HQBPF disabled.

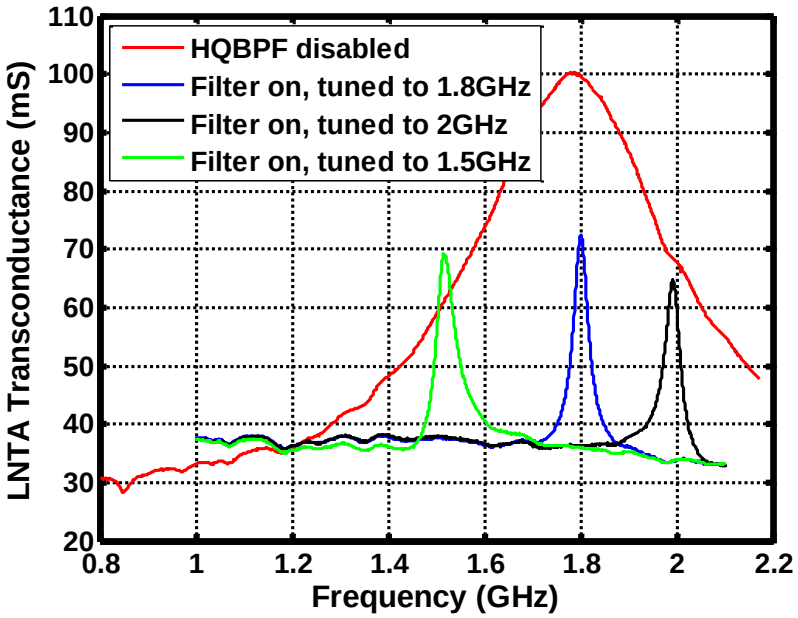


Figure 4.16: Measured LNTA transconductance.

achieve lower NF (≈4.5 dB from the simulation and XX dB from the measurement). The measured S_{11} is plotted in Figure 4.17 showing a good 50-Ω impedance matching (S_{11}<-10 dB) for the frequencies between 0.8 to 2.2 GHz, which proves the wideband impedance matching property of the implemented LNTA.

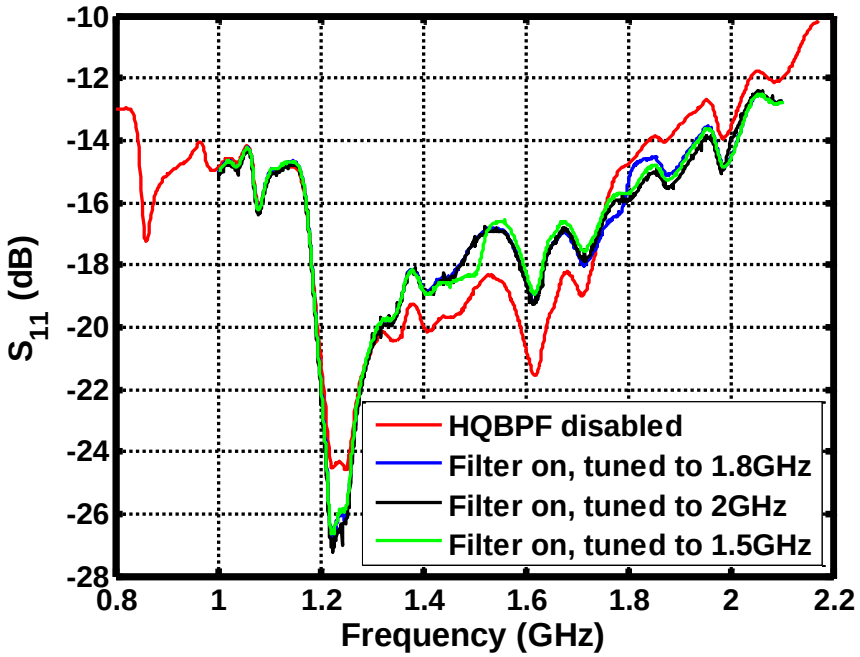


Figure 4.17: Measured S_{11}.

4.3.2 Noise Measurement Results

For noise measurements, the LNTA was tuned to 1.8 GHz. The measurement result shows an overall in-band NF of 8.8 dB (7.6 dB from simulation), which also includes the buffer stage and the termination resistor noise. By de-embedding their noise using (4.1), the LNTA noise figure becomes approximately equal to 6.5 dB (4.9 dB from simulation). The discrepancy can partly arise from the in-band gain reduction and partly from the

4.3.3 Desensitization Measurement Results

The resilience of the LNTA against blockers was measured by means of the blocker compression in Figure 4.18. The LNTA is tuned to 1.8 GHz. A CW wanted signal was located in-band (i.e. at 1.8 GHz) and a CW blocker was located at 100 MHz offset frequency (i.e. 1.9 GHz). The power of the blocker was swept and the small-signal gain change of the in-band signal was measured and plotted. The expansive/compressive behavior of the LNTA is obvious in Figure 4.18. The effect of such behavior in IMD cancellation is shown in section 4.3.4.

It can also be seen that the overall (LNTA and buffer stage) -1-dB desensitization point is around

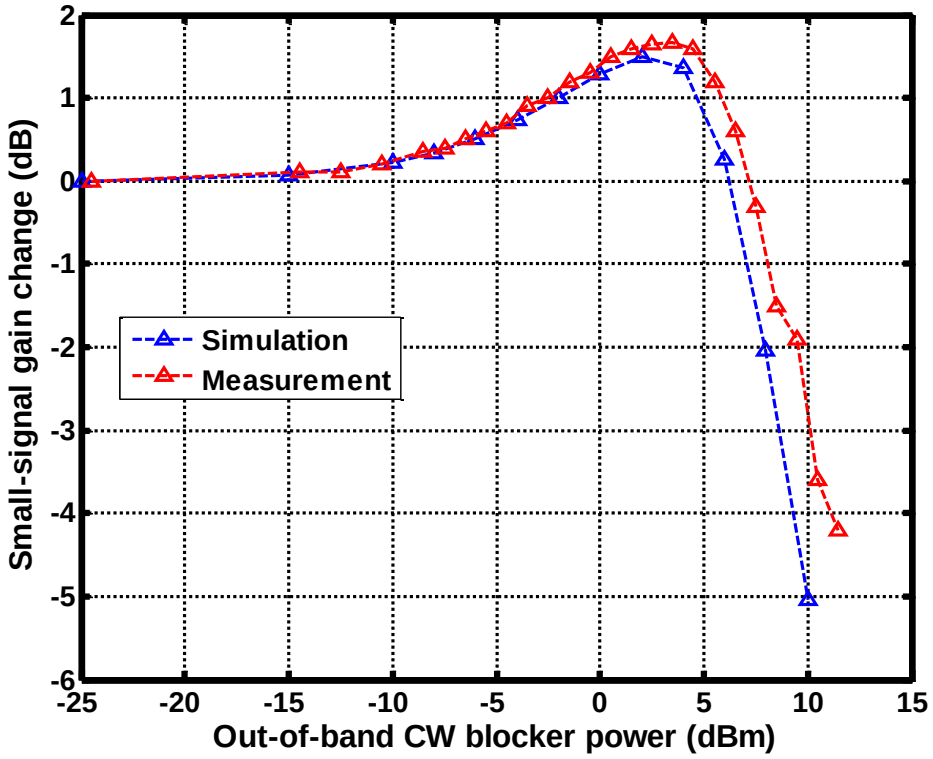


Figure 4.18: Measured vs. simulated small-signal gain change for a CW large blocker at 100 MHz frequency offset.

+7 dBm, which is very large. In comparison to the simulation results (section 0), the maximum gain expansion has increased by almost +0.2 dB, which can be justified by the reduction in the in-band gain. In addition, according to the simulations, the output buffer compression reduces the actual -1-dB desensitization point of the LNTA by almost 1 dB. Therefore, the -1-dB desensitization point of the LNTA can be approximated to be around +8 dBm.

It should be emphasized here that the implemented LNTA comprise a single-ended topology. The 1-dB desensitization point can be improved by around 3 dB by using a differential topology.

4.3.4 Intermodulation Measurement Results

To characterize the linearity performance of the LNTA, the in-band 3rd order IMD products were measured, which are shown in Figure 4.19. For linearity measurements, the buffer stage was set to low-gain mode and the LNTA was tuned to 1.8 GHz. Two CW signals were placed in-band at 1800.6 MHz with 200 kHz spacing. The IMD product at 1800.3 MHz was then measured and used for IIP_3 extrapolation, which is plotted in Figure 4.20.

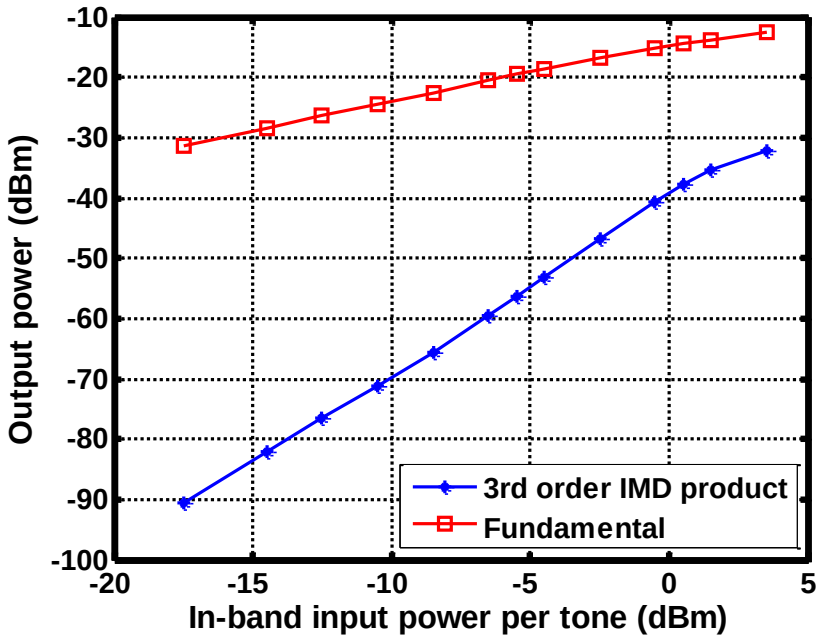


Figure 4.19: Measured P_{in}-P_{out} fundamental and IMD curves for two in-band CW signals.

The out-of-band IIP_3 (OB-IIP_3) of the LNTA was also measured by applying two CW blockers with equal powers at 1900 MHz and 1999 MHz. The LNTA was tuned to 1.8 GHz and the in-

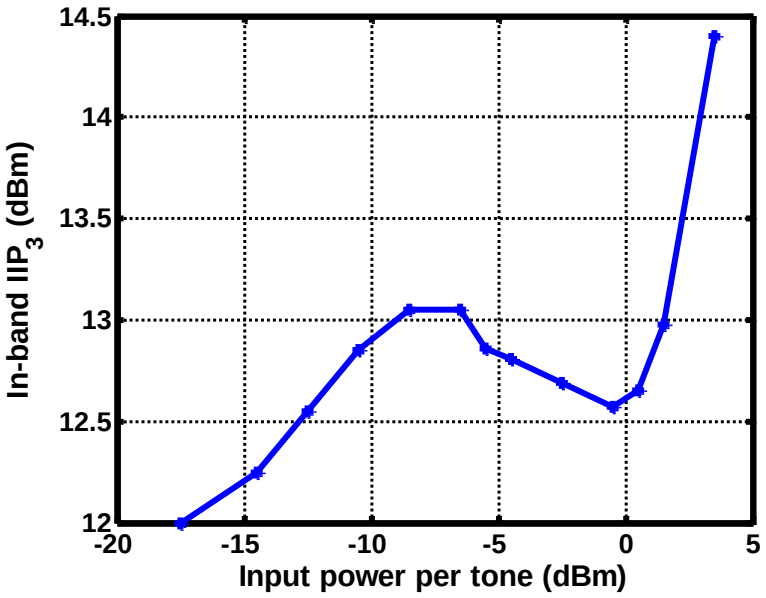


Figure 4.20: Measured in-band IIP3.

band IMD product at 1801 MHz was referred to the input using small-signal in-band gain (see section 4.3.1) and was used to extrapolate OB-IIP_3 according to

$$IIP_3 = P_{in} + \frac{P_{in} - IMD3_{in,referred}}{2} \tag{4.3}$$

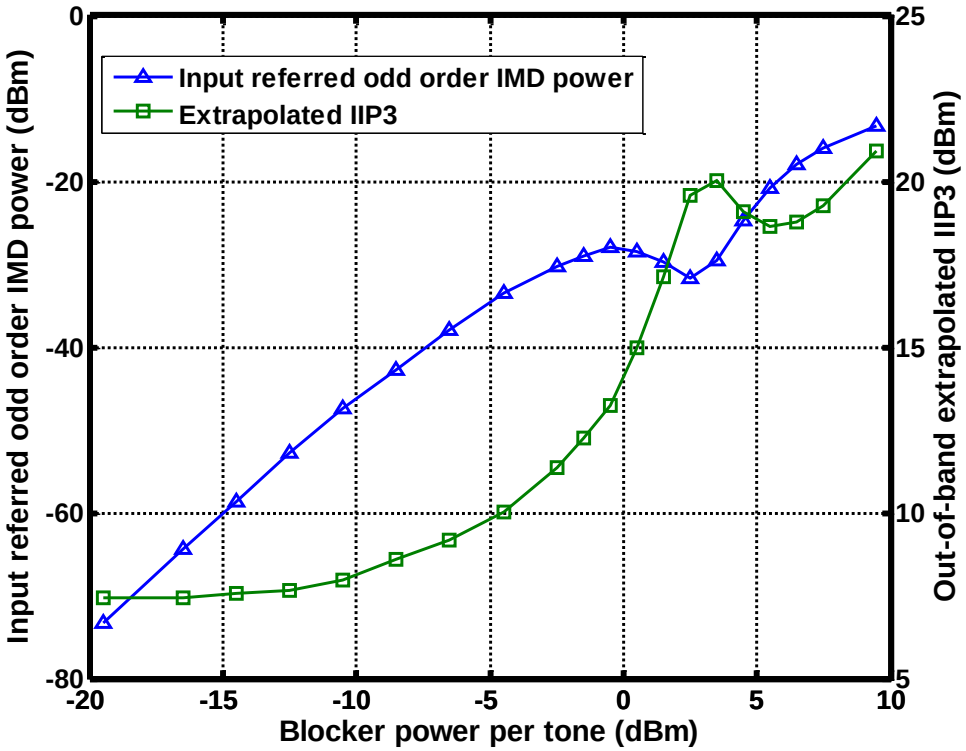


Figure 4.21: Measured extrapolated out-of-band IIP3.

where P_{in} is the power of the out-of-band CW signals and $IMD3_{in,referred}$ is the input-referred power of the in-band odd order IMD products. The result is plotted in Figure 4.21. The comparison between the simulated (see section 3.3.4) and the measured results is plotted in Figure 4.22. It can be seen that the results agree well.

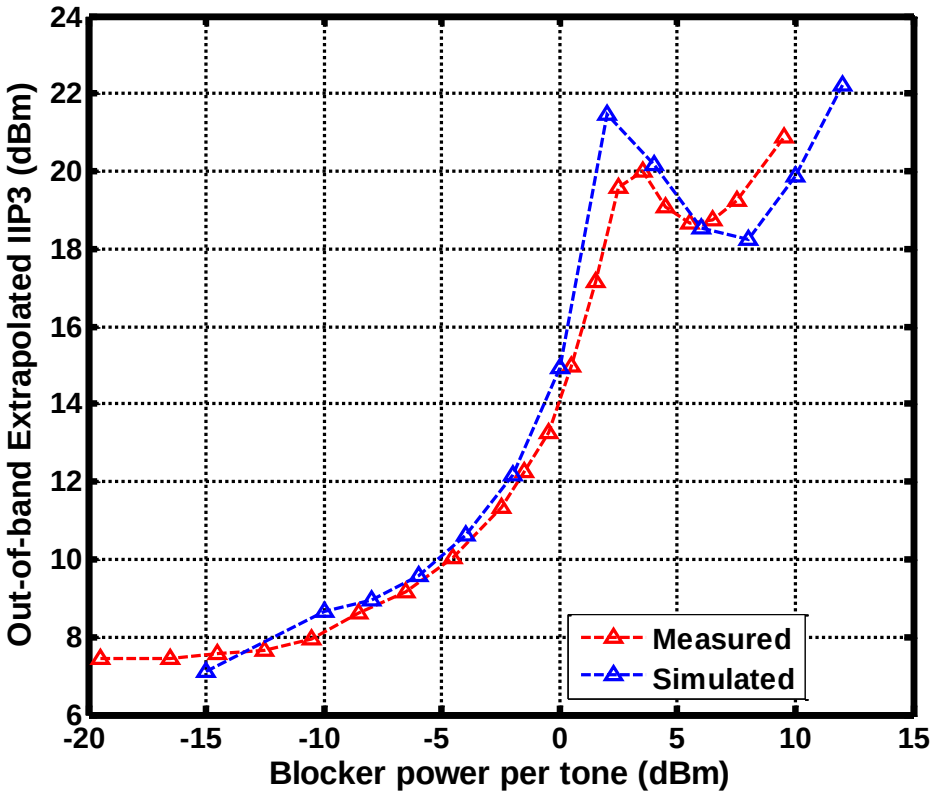


Figure 4.22: Comparison of the simulated and measured extrapolated OB IIP_3.

4.3.5 LO-to-RF Leakage

Due to the drain-source capacitance of the transistors and their finite r_o, the LO leakage through the HQBPFs can reach to the input and, eventually leak into the antenna, which is undesirable. For example, the 3GPP specifies that the LO leakage to the antenna should be less than -36 dBm [6]. For the proposed LNTA, the LO leakage to the input was less than -90 dBm from both the simulations and measurements, which is well below the specifications.

4.4 Comparison to State-of-the-Art

The measured performance of the proposed LNTA is summarized in Table 4.2 and compared to state-of-the-art. According to the table, this work therefore reports the LNTA with a large blocker tolerance and moderate noise performance using a single-ended topology and 1.5 V supply voltage.

Parameter	This work	[37]	[5]	[24]	[29]
System	Measured LNTA	Simulated LNTA	Simulated LNTA	Simulated LNTA	Measured LNTA
RF input	Single-ended	differential	differential	differential	differential
Technology (nm)	65	65	65	90	45
Band of operation (GHz)	0.8-2.2	Up to 6	GSM850/PCS	2.14	0.1-2
g_m (mS)	75/100[1]	50 (full-circuit)	60 (full-circuit)	20 (full-circuit)	36.5
Matching gain[5] (dB)	+17	+11	+12.5	+3	+8.2
NF (dB)	6.5/5.9[1]	<3	1.4	1.8/10.7[3]	4.5 (at 2GHz)
Blocker NF (dB) @ Blocker power (dBm)	10.3 @ +5	—	8 @ 0[6]	4.5 @ +5	—
In-band IIP3 (dBm)	+12	+3.5	0[6]	—	+10
Out-of-band IIP3 (dBm)	+7.5 (SSIIP3) +20 (LSIIP3)[2]	+16	—	+15.5 (SSIIP3) +32.8 (LSIIP3)	—
1-dB compression point (dBm)	—	+4	—	—	0 (R_L=30Ω)
1-dB desensitization point (dBm)	+8 (R_L=10Ω)	<+1 (B_{1dB}<P_{1dB}-3)	+1	+22 (R_L=0Ω)	<-3 (B_{1dB}<P_{1dB}-3)
Current (mA)	7.5	14	8	5.4[4]	16
Supply Voltage (V)	1.5	1.2	2.5	1.5	2.2

[1]on-chip high-Q bandpass filters are disabled
[2]large-signal IIP3
[3]complete RX NF (due to small g_m, overall RX NF is large [32]).
[4]including biasing
[5]matching gain is defined as $10\log(g_{m,\,fullcircuit}^2 R_L R_s)$ with R_L=100 Ω and R_s=50 Ω
[6]complete RX

Table 4.2: The proposed LNTA performance summary and comparison to state-of-the-art.

Chapter 5

CONCLUSIONS AND FUTURE WORK

In this work, a very linear LNTA capable of large-signal handling for current-mode RX front-end was proposed and implemented in 65-nm CMOS process. It was shown that by combining the on-chip high-Q bandpass filters with a push/pull common-gate stage, a large desensitization point of +8 dBm with moderate NF of 5.9 dB can be achieved. In addition, the large in-band g_m of the LNTA (≈100mS) provides sufficient suppression of the noise from the stages following the LNTA.

To further improve the performance of the proposed LNTA the following modifications and consideration can be applied in the future design:

1) A differential topology should be used to further enhance the large-signal handling of the LNTA.

2) To improve the NF, the load impedance of the push/pull common-gate stage can be increased by choosing a lager value for the inductance (currently it is around 4 nH). This way R_{tot}, hence the in-band impedance of the HQBPFs increases, which can reduce NF according to (3.43).

Moreover, the in-band impedance of the HQBPFs can be increased by using less sharp edges for the 25% duty-cycle LO clocks (see section 3.3). This way, not only the digital circuitry power consumption can be reduced, but also in-band impedance of the HQBPFs, hence the NF, can be improved.

3) A capacitor tank can be used for the LC tank in parallel with the HQBPFs, to tune the resonance frequency of the tank to the desired ω_{LO}, to achieve wide-band operation, while maintaining the maximum out-of-band rejection in the frequency response of the LNTA.

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