A time-to-digital system, such as a frequency synthesizer, includes a power management circuit and a time-to-digital converter (TDC). Said power management circuit is coupled to a frequency reference clock and a variable clock, and arranged to output a delayed frequency reference clock and a single pulse of said variable clock ahead of a transition of said delayed frequency reference clock. Said TDC is coupled to said power management circuit and arranged to produce a digital TDC output.
FIG. 1
FIG. 2

e[k] = 1 - (tr/Tv)

code edge detector

TDC

REF_in

TDC_in

REF_in

16a

Tv

t

Dt

16b

e[k] = 1 - (tr/Tv)

16c
FIG. 3

Reference phase accumulator

Variable phase accumulator

Loop filter

Shift controller

Phase shifter

TDC

TDC_in

REF_in

CKR

FREF

FCW

PHR[k]

PHF[k]

PHF1[k]

PHF2[k]

1/Tv_avg

et[k]

OTW

CKV

FIG.

32a

34

32b

30

10

42

46

40

38

1

0
FIG. 4

\[ \text{time} \]

\[ (-e[k]) = (-e[k]) + \text{PHF} \]

\[ \text{PHF} [k] \]

\[ \text{PHF2} [k] \]

\[ FREF \]

\[ CKW \]

\[ CKV \]

\[ t \]

\[ e[k] \]

\[ 1-e[k] \]
FIG. 6
FIG. 7
FIG. 12
TIME-TO-DIGITAL SYSTEM AND ASSOCIATED FREQUENCY SYNTHESIZER

This application claims the benefit of U.S. provisional application Ser. No. 61/548,096, filed Oct. 17, 2011, the subject matter of which is incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates to frequency synthesizer, and more particularly, to frequency synthesizer including peripheral mechanism supporting time-to-digital conversion with improvement of reduced hardware complexity, lower power consumption, suppressed supply interference, reduced layout area and enhanced linearity, etc.

BACKGROUND OF THE INVENTION

Various communication systems, such as wireless communication systems of radio frequency (RF), are broadly adopted and play an important role in modern information society. A core technique for modern communication systems is frequency (and/or clock) synthesis, which generates a variable clock of a desired frequency based on a frequency reference clock, such that stability, accuracy, and spectral purity of the variable clock correlate with performance of the frequency reference clock. In a transmitter, the variable clock provided by a local frequency synthesizer can be utilized as a local oscillation carrier for an up-conversion frequency translation from baseband or intermediate-frequency (IF) signals to RF signals. On the other hand, in a receiver, the variable clock provided by a local frequency synthesizer can be adopted as a local oscillation carrier for a down-conversion from RF signals to IF/baseband signals.

SUMMARY OF THE INVENTION

A frequency synthesizer accepts a frequency reference clock and a frequency command word (FCW) for input, and outputs a variable clock in response, such that a frequency of the variable clock is an FCW multiple of the frequency reference clock. A high-speed variable clock of frequency in an order of GHz can therefore be generated based on a stable low-speed frequency reference clock of frequency in an order of tens of MHz, for example.

An embodiment of the invention provides a time-to-digital system, such as a frequency synthesizer, including a frequency reference input for receiving a frequency reference clock, a variable clock input for receiving a variable clock of higher frequency than said frequency reference clock, a power management circuit and a time-to-digital converter (TDC). Said power management circuit is coupled to said frequency reference input and said variable clock input, and arranged to output a delayed frequency reference clock and a single pulse of said variable clock at a transition of said delayed frequency reference clock. Said TDC is coupled to said power management circuit for producing a digital TDC output.

In an embodiment, said power management circuit includes a first logic gate, a delay and a second logic gate. Said first logic gate is coupled to said frequency reference clock and said delayed frequency reference clock, and arranged to provide a gating signal in response to a first logic operation result of said frequency reference clock and said delayed frequency reference clock. Said delay is coupled to said frequency reference clock and said first logic gate for providing said delayed frequency reference clock by delaying said frequency reference clock. Said second logic gate is coupled to said gating signal and said variable clock for providing said single pulse of said variable clock in response to a second logic operation result of said variable clock and said gating signal.

When said frequency reference clock transits from a first level (e.g., a level of logic 0) to a second level (a level of logic 1), said first logic gate is arranged to set said gating signal to said second level; when said delayed frequency reference clock subsequently transits from said first level to said second level, said first logic gate is arranged to set said gating signal to said first level. When said gating signal is of said first level, said second logic gate is arranged to suppress pulses of said variable clock; and when said gating signal is of said second level, said second logic gate is arranged to provide said single pulse of said variable clock by tracking said variable clock.

In an embodiment, said power management circuit includes a first logic gate, a delay, a level sense circuit and a second logic gate. Said first logic gate is coupled to said frequency reference clock and said delayed frequency reference clock and said first logic gate for providing said delayed frequency reference clock by delaying said frequency reference clock. Said delay is coupled to said frequency reference clock and said first logic gate for providing said delayed frequency reference clock by delaying said frequency reference clock. Said level sense circuit is arranged to set said second gating signal to said first level. In an embodiment, said level sense circuit includes a latch.

When said frequency reference clock transits from a first level to a second level, said first logic gate is arranged to set said first gating signal to said second level, and when said delayed frequency reference clock subsequently transits from said first level to said second level, said first logic gate is arranged to set said first gating signal to said first level. When said first gating signal transits from said first level to said second level while said variable clock is of said first level, said level sense circuit is arranged to set said second gating signal to said second level, and when said first gating signal transits from said first level to said second level while said variable clock is of said second level, said level sense circuit is arranged to set said second gating signal to said second level when said variable clock transits back to said first level.

When said second gating signal is of said first level, said second logic gate is arranged to suppress pulses of said variable clock; and when said second gating signal is of said second level, said second logic gate is arranged to provide said single pulse of said variable clock by tracking said variable clock. Said level sense circuit is also arranged to set said second gating signal to said first level when said first gating signal transits to said first level. In an embodiment, said level sense circuit includes a latch.

In an embodiment, said time-to-digital system further comprises a phase shifter and an oscillator such that said time-to-digital system functions as a frequency synthesizer. Said phase shifter is coupled to said power management circuit, and arranged to adjust a time difference between a transition of said frequency reference clock and a subsequent transition of said variable clock, such that said time difference is less than a period of said variable clock. Said oscillator is coupled to said variable clock input for tuning periods of said variable clock according to said digital TDC output.

In an embodiment, said time-to-digital system further comprises a phase shifter and an oscillator such that said time-to-digital system functions as a frequency synthesizer. Said phase shifter is coupled to said power management circuit, and arranged to adjust a time difference between a transition of said frequency reference clock and a subsequent transition of said variable clock, such that said time difference is less than a period of said variable clock. Said oscillator is coupled to said variable clock input for tuning periods of said variable clock according to said digital TDC output.
An embodiment of the invention provides a frequency synthesizer including a power management circuit, a TDC, an oscillator, a phase shifter and a shift controller. Said power management circuit is arranged to output a second reference clock and a second variable clock in response to a first reference clock and a first variable clock, such that a single pulse between a transition of said first reference clock and a subsequent transition of said second reference clock is provided in said second variable clock. Said TDC is coupled to said power management circuit, and arranged to provide a first fractional error correction signal by quantizing a time difference between said second reference clock and said second variable clock.

In an embodiment, said shift controller is coupled to said phase shifter, and arranged to provide a shift control signal and a second fractional error correction signal in response to an accumulated value of FCW. Said oscillator is further arranged to tune periods of said first variable clock according to said first fractional error correction signal and said second fractional error correction signal.

In an embodiment, said oscillator is arranged to provide an original variable clock. Said phase shifter is coupled between said oscillator and said power management circuit, and arranged to provide said first variable clock by shifting said original variable clock, such that a time difference between a transition of said first reference clock and a transition of said first variable clock is less than a period of said original variable clock. Said phase shifter is arranged to adjust a phase offset between said original variable clock and said first variable clock in response to said shift control signal.

In an embodiment, said power management circuit includes a first logic, a delay and a second logic. Said first logic is coupled to said first reference clock and said second reference clock, and arranged to provide a gating signal in response to a first logic operation result of said first reference clock and said second reference clock. Said delay is coupled to said first reference clock and said first logic gate for providing said second reference clock by delaying said first reference clock. Said second logic gate is coupled to said gating signal and said first variable clock for providing said second variable clock in response to a second logic operation result of said first variable clock and said gating signal.

When said first reference clock transits from a first level to a second level, said first logic gate is arranged to set said first gating signal to said second level, and when said second reference clock subsequently transits from said first level to said second level, said first logic gate is arranged to set said first gating signal to said first level. When said first gating signal transits from said first level to said second level while said first variable clock is of said first level, said level sense circuit is arranged to set said second gating signal to said second level; and when said first gating signal transits from said first level to said second level while said first variable clock is of said second level, said level sense circuit is arranged to set said second gating signal to said second level when said first variable clock transits back to said first level.

When said second gating signal is of said first level, said second logic gate is arranged to suppress pulses of said second variable clock; and when said second gating signal is of said second level, said second logic gate is arranged to provide said single pulse of said second variable clock by tracking said first variable clock.

Numerous objects, features and advantages of the present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description of embodiments of the present invention when taken in conjunction with the accompanying drawings. However, the drawings employed herein are for the purpose of descriptions and should not be regarded as limiting.

BRIEF DESCRIPTION OF THE DRAWINGS

The above objects and advantages of the present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description and accompanying drawings, in which:

FIG. 1 illustrates an embodiment of digitally tracking phases of a variable clock and a frequency reference clock;
FIG. 2 illustrates an embodiment of a TDC;
FIG. 3 and FIG. 4 respectively illustrate a frequency synthesizer and its operation according to an embodiment of the invention;
FIG. 5 and FIG. 6 respectively illustrate a frequency synthesizer and its operation principle according to an embodiment of the invention;
FIG. 7 and FIG. 8 respectively illustrate a frequency synthesizer and its operation according to an embodiment of the invention;
FIG. 9 illustrates a frequency synthesizer according to an embodiment of the invention;
FIG. 10 illustrates an embodiment of the power management circuit in FIG. 9 according to the invention;
FIG. 11 illustrates an embodiment of the power management circuit in FIG. 9 according to the invention;
FIG. 12 illustrates operation examples of the power management circuit in FIG. 11 according to an embodiment of the invention; and FIG. 13 illustrates an implementation example of the level sense circuit in FIG. 11 according to an embodiment of the invention.

**DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS**

Please refer to FIG. 1 illustrating a conceptual embodiment for digitally tracking phases of a clock CKV and a clock FREE, such that frequency of the clock CKV is an FCW multiple of frequency of the clock FREE. That is, by assigning a corresponding FCW, a clock CKV of a desired frequency is produced based on a clock FREE. The clock FREE is a frequency reference clock of a period Tr. The clock CKV, generated by an oscillator 10, e.g., a digitally controlled oscillator (DCO), is a variable clock of a period Tr. For frequency synthesis, the oscillator 10 is tuned so that the clock CKV locks to the clock CKR, so frequency of the clock CKV approaches FCW multiple the clock FREE in the limit, i.e., the average period Tr equals TV/FCW. The FCW is in general an integer since it accumulates integers.

While digitally representing phase of the clock CKV, a signal (e.g., a digital word) PHV[i] is provided. The signal PHV[i], as a variable phase signal, accumulates a unit count at every significant transition (e.g., rising edge) of the clock CKV, i.e., PHV[i+1]=PHV[i]+1 with index i indicating a time stamp of the i-th significant transition of the clock CKV. That is, as time progresses, the variable phase signal PHV[i] accumulates a count of periods of the clock CKV to reflect phase of the clock CKV in terms of the period Tr. The signal PHV[i] is an integer since it accumulates integers.

As the time stamp k progresses, the difference (PHV[k]-PHR[k]) between the signals PHV[k] and PHR[k] varies from (3-9/4)=314. Similarly, at the time stamp (k+2), the "misalignment" of (3/4)*TV between the significant transitions of the clock FREE and CKV is reflected by (PHV[k+2]-PHR[k+2])=(314/2-14/4)=4=(3/4).

The regular misalignment between the significant transition of the clock FREE and the subsequent significant transition of the clock CKV is in a range of one period TV; equivalently, the difference (PHV[k]-PHR[k]), which leads to the deterministic part of the error e[k], is a fractional number in general (or equal to zero). Since the signal PHV[k] is an integer, the deterministic part of the error e[k] is related to the fractional part of the PHR[k]. For practical application, the error e[k] also includes a fluctuating part of random nature, reflecting stochastic phase error due to noise of the oscillator 10, etc.

To be more general, let the FCW be expressed by NV/Nr, e.g., a flip-flop. The re-timer 12 is arranged to provide the re-timed reference clock CKR by re-timing the clock FREE at significant transitions of the clock CKV, such that each transition of the clock CKR aligns with a significant transition of the clock CKV. In response to triggering of the clock CKR, a signal PHR[k] is provided to digitally reflect phase of the clock FREE. The signal PHR[k], as a reference phase signal, accumulates the FCW at every significant transition of the clock CKR, i.e., PHR[k+1]=PHR[k]+FCW, with index k indicating a time stamp of the k-th significant transition of the clock CKR. The FCW is in general an integer since it accumulates integers.

As the period Tr of the clock FREE is expected to be an FCW multiple of the period TrV of the clock CKV, accumulating FCW on each period of the clock CKR is used to reflect phase of the clock FREE in terms of the period TV. Since the FCW generally has a fractional part, the signal PHR[k] also has a fractional part in general.

Because the clock CKR is re-timed by the clock CKV, each significant transition of the clock CKR aligns with a significant transition of the clock CKV, then the signal PHV[k], i.e., the signal PHV[k] at k-th significant transition of the clock CKR, can be compared with the signal PHR[k]. In the example of FIG. 1, the signal PHV[10] aligns with the signal PHR[10], and the signal PHV[0+5]-PHV[0+1] synchronizes with the signal PHR[0+1], etc. As shown in FIG. 1, re-timing the clock FREE to the clock CKR by triggering of the clock CKV induces an error e[k], representing a time difference (phase error) between a significant transition of the clock FREE and a subsequent significant transition (i.e., the closest significant transition after the significant transition of the clock FREE) of the clock CKV.

In the example of FIG. 1, when the clock CKV locks the clock FREE with the desired relation TV=Tr/FCW, four every cycles of the period Tr will align with every nine cycles of the period TV, since FCW=9/4. That is, accumulating the FCW four times equals accumulating the unit count nine times, for FCW*4=(9/4)*4=9. Assuming the significant transitions of the clocks FREE and CKV align at the time stamp k0 such that the values of the signals PHR[k0] and PHV[k0] are equal, then, after four cycles of the clock CKR, the significant transitions of the clocks FREE and CKV align again, and the value of the signal PHR[k0+4] also meets the value of the signal PHV[k0+4] (i.e., PHV[k0+4]-9/4) because PHR[k0+4]-PHR[k0]+FCW*4, and PHV[k0+4]-PHV[k0]+1. On the other hand, owing to the fractional part of the FCW, the time difference between a significant transition of the clock FREE and a subsequent significant transition of the clock CKV is non-zero at each time stamp k between the time stamps k0 and (k0+4) even when the clock CKV locks to the clock FREE, and the time difference is reflected by an arithmetic difference between the signals PHV[k] and PHR[k]. For example, at the time stamp (k0+1), the significant transition of the clock FREE is ahead of the subsequent significant transition of the clock CKV by (3/4)*TV when the clock CKV locks the clock FREE, and the arithmetic difference between PHR[k0+4]-PHR[k0] indicates the time difference (PHV[k0+4]-PHR[k0+1])-(3/4)-4. Similarly, at the time stamp (k0+2), the "misalignment" of (3/4)*TV between the significant transitions of the clock FREE and CKV is reflected by (PHV[k0+2]-PHR[k0+2])=(3/4)2/4=(3/4)

As the time stamp k progresses, the difference (PHV[k]-PHR[k]) between the signals PHV[k] and PHR[k] varies regularly and periodically, and reflects a deterministic time difference (phase error) between (the significant transitions of the clocks FREE and CKV in terms of the period TV. Hence, the difference (PHV[k]-PHR[k]) becomes a deterministic part of the error e[k], reflecting a regular phase error due to the fractional part of the FCW. That is, when the clock CKV locks the clock FREE, the error e[k] equals (PHV[k]-PHR[k]), or PHR[k+e[k]-PHV[k]]=0.

The regular misalignment between the significant transition of the clock FREE and the subsequent significant transition of the clock CKV is in a range of one period TV; equivalently, the difference (PHV[k]-PHR[k]), which leads to the deterministic part of the error e[k], is a fractional number in general (or equal to zero). Since the signal PHV[k] is an integer, the deterministic part of the error e[k] is related to the fractional part of the PHR[k]. For practical application, the error e[k] also includes a fluctuating part of random nature, reflecting stochastic phase error due to noise of the oscillator 10, etc.
variable clock at the time of the rising edge \( t_r \). That

a plurality of flip-flops 24 triggered by the signal

et\( [k] \). The TDC 20 is therefore adopted to digitally detect the error \( e[k] \) every cycle of the clock CKR, so the oscillator 10 can be tuned according to a digital TDC output of the TDC to ensure \( (PHR[k]+e[k]−PHV[k]) \) approaches zero at each time stamp.

Please refer to FIG. 2 illustrating an embodiment of a TDC 20. The TDC 20 is coupled to two inputs 22a and 22b for respectively receiving two signals TDC_in and REF_in, and outputs a signal et[k] as a digital TDC output. While the TDC 20 is adopted to detect the error \( e[k] \) shown in FIG. 1, the clocks FRE and CKV are respectively received as the signals REF_in and TDC_in. The TDC 20 is arranged to preferably quantize a time difference \( dt \) between a significant transition \( 16b \) of the signal REF_in and a subsequent transition \( 16c \) of the signal TDC_in, thus the error \( e[k] \) is represented by the digital signal et[k]. In an embodiment, the TDC 20 is a causal system; hence it cannot ‘see’ the next edge \( 16c \) of the variable clock at the time of the rising edge \( 16b \) of REF_in clock. Consequently, the desired measurement is performed indirectly by subtracting a time \( t_r \) value from the period \( T\)v.

In an embodiment, the rising time \( t_r \) between a significant transition \( 16a \) of the signal TDC_in and the subsequent significant transition \( 16b \) of the signal REF_in measured and quantized; since \( dt = (T\)v−\( t_r \)), the error \( e[k] \) is derived as \( e[k]=(-dt)/(T\)v−1/(T\)v_avg)). Note that, in the direct TDC output, the quantized value of \( t_r \) is then divided by the frequency \( T\)v period or multiplied by \( 1/(T\)v_avg). Hence, the direct TDC output is a quantized value of \( t_r \), which corresponds to a negative of the error \( e[k] \). It should be appreciated by one skilled in the art that the negative operation is essentially achieved by inverting a sign of the adder 50 input (discussed in FIG. 3). Hence, minimizing \( t_r \), which is the timing separation between the TDC 20 inputs REF_in and TDC_in, is equivalent to maximizing \( e[k] \) (which cannot be greater than 1). Since the constant \( 1^1 \) in \( 1-e[k] \) is easily absorbed in the PLL system, \( 1-e[k] \) can be conveniently denoted as \( -e[k] \). This way the timing separation between the significant transition \( 16b \) of the signal REF_in and the following significant transition \( 16c \) of the signal TDC_in (denoted as \( e[k] \)) and the prior significant transition \( 16a \) of the signal TDC_in (denoted as \( -e[k] \)) can be both used depending on convenience.

An embodiment of the TDC 20 includes a plurality (e.g., a number \( L \)) of serially connected delay units 18 (e.g., inverters), a plurality of flip-flops 24 triggered by the signal REF_in, and a code edge detector 26. Each delay unit 18 imposes a unit delay time \( t\) inv to the signal TDC_in, and outputs the delayed signal to a corresponding flip-flop 24 and a next delay unit 18. When the significant transition of the signal REF_in triggers the flip-flops 24 to obtain a code of bits Q(1), Q(2), Q(3),..., Q(L), occurrence of the significant transition \( 16c \) is reflected by a code edge in the code of the bits Q(1) to Q(L), and the rise time \( t_r \) is quantized in terms of the unit delay time \( t\) inv by the code edge detector 26 and outputted as the signal et[k]. That is, a time quantization resolution of the TDC 20 is determined by the unit delay time \( t\) inv of each delay unit 18. The total number \( L \) of the delay unit 18 determines a measuring range (a TDC range) of the TDC 20; the TDC range of the TDC is approximately \( L\cdot t\) inv. A time interval shorter than the TDC range can be measured, and a time interval longer than the TDC range is not detected by the TDC 20. While the TDC 20 is used to detect the error \( e[k] \) shown in FIG. 1, the TDC range should cover a full range of the period \( T\)v.

To detect the error \( e[k] \) in finer resolution for better quality of the clock CKV, the unit delay time \( t\) inv is set much shorter than the period \( T\)v. Consequently, the TDC 20 needs a much larger number \( L \) of the delay unit 18 to cover a TDC range of the period \( T\)v. For example, to cover a period of 2.4 GHz with 7 ps resolution, about sixty delay units 18 are applied to implement the TDC 20. As more delay units 18 are adopted, more power is consumed, and more supply interference (e.g., fluctuation and/or drop of supply voltages) is induced. To settle high supply interference, decoupling capacitors of large area must be utilized, and area to implement an effective TDC is therefore increased. Moreover, high supply interference degrades linearity of time-to-digital conversion, since amount of the unit delay time \( t\) inv drifts when supply voltages fluctuate. Therefore, supporting peripherals to reduce required delay units and to enhance linearity of TDC are demanded.

Please refer to FIG. 3 illustrating a frequency synthesizer 30 according to an embodiment of the invention. The frequency synthesizer 30 has an FCW input 32a for receiving FCW, a frequency reference input 32b for receiving a frequency reference clock FRE, a reference phase accumulator 34, a variable phase accumulator 36, a loop filter 38, an oscillator 10, a phase shifter 46, a shift controller 42, a TDC 20, an adder 50 and a re-timer 12. The oscillator 10 is arranged to provide a variable clock CKV, e.g., an RF clock, in response to an oscillator tuning word (OTW), such that the frequency of the variable clock CKV is FCW multiple of the frequency reference clock FRE when the variable clock CKV locks to the frequency reference clock FRE.

The re-timer 12 is coupled to the oscillator 10 and the frequency reference clock FRE, and arranged to provide a re-timed frequency reference clock CKR by re-timing the frequency reference clock FRE at significant transitions (e.g., rising edges) of the variable clock CKV. The reference phase accumulator 34 is coupled to the frequency reference clock FRE through the frequency reference input 32b, and arranged to provide a reference phase signal PHR[k] by accumulating the FCW in response to each period of the frequency reference clock FRE, e.g., at significant transitions of the re-timed reference clock CKR. In FIG. 3, the reference phase signal PHR[k] is decomposed to a fractional part PHR[k] and an integer part PHR[k]. The variable phase accumulator 36 is coupled to the oscillator 10, and arranged to provide a variable phase signal PHV[k] by accumulating a count of periods of the variable clock CKV.

The phase shifter 46 is coupled to the oscillator 10 and the shift controller 42, and arranged to provide a shifted variable clock CKV' by changing phase of the variable clock CKV in response to a shift control signal SEL. Alternatively, the phase shifter 46 could perform phase changing by selecting one of a multiple of CKV phases. The generation of the multiple phases could be done internally to the phase shifter 46. The TDC 40 functions similar to the TDC 20 shown in FIG. 2; the TDC 40 is coupled to the phase shifter 46 and the frequency reference input 32b, arranged to receive the frequency reference clock FRE and the shifted variable clock CKV' as the signals REF_in and TDC_in, and arranged to provide a fractional error correction signal PHIF[k] in response to a time difference between the frequency reference clock FRE and the shifted variable clock CKV'. That is, the TDC 40 is arranged to detect (quantize) the time difference between a significant transition of the frequency reference clock FRE and a subsequent significant transition of the shifted variable

...
clock CKV', and provide a signal et[k] to reflect the detected time difference; then the fractional error correction signal PHF1[k], indicating the time difference in terms of the period Tv of the variable clock CKV, is provided by normalizing the signal et[k] to an averaged period TTV_avg, which is a long-term average of the periods of the variable clock CKV, since the period TTV is in general a time-varying value.

To cooperate with the phase shifter 46, the shift controller 42 is coupled to the phase shifter 46 and arranged to provide the shift control signal SEL and another fractional error correction signal PHF2[k]. The adder 50 is coupled to the variable phase accumulator 36, the reference phase accumulator 34, the shift controller 42 and the TDC 40, and arranged to provide a signal PHF1[k] in response to an arithmetic combination (PHR[k]-PHF2[k]-PHV[k]) of the reference phase signal PHR[k], the variable phase signal PHV[k], and the fractional error correction signals PHF1[k] and PHF2[k]. The loop filter 38 is coupled between the oscillator 10 and the adder 50, and arranged to provide the OTW in response to the signal PHF1[k]. Thus, through the OTW, the oscillator 10 is arranged to tune periods of said variable clock CKV according to the reference phase signal PHR[k], the variable phase signal PHV[k] and the fractional error correction signals PHF1[k] and PHF2[k].

Please refer to FIG. 4 illustrating TDC operation of the frequency synthesizer 30 according to an embodiment of the invention. The phase shifter 46 (FIG. 3) is arranged to induce a phase offset PHoffset between the variable clock CKV and the shifted variable clock CKV'. With the phase offset PHoffset, the error (1-ε)[k] between the frequency reference clock FREF and the previous variable clock CKV is decreased to a smaller error (1-ε)[k], i.e., decreased the timing separation between the frequency reference clock FREF and the shifted variable clock CKV', with ε[k]-ε[k+PHoffset]. In other words, the phase offset PHoffset is such arranged that a time difference between a significant transition of the frequency reference clock FREF and a previous significant transition of the shifted variable clock CKV' is significantly less than a period Tv of the variable clock CKV; i.e., the error ε[k] never grows larger than a portion of the period Tv. As the shifted variable clock CKV' and the frequency reference clock FREF are respectively received as the signals TDC_in and REF_in, the TDC 40 only needs to quantize the error ε[k] significantly shorter than the period Tv. In other words, the TDC range of the TDC 40 just needs to cover a portion of one period Tv, instead of full range of the period Tv. The TDC 40 is arranged to respond only when a significant transition of the shifted variable clock CKV' and a significant transition of the frequency reference clock FREF occur in a proximity of the TDC range; the TDC 40 does not have to respond when significant transitions of the shifted variable clock CKV' and significant transitions of the frequency reference clock FREF do not occur in a proximity of the TDC range. Since the required TDC range is decreased, the TDC 40 benefit from lower quantity of required delay units; hardware complexity, power consumption, layout area, supply interference and linearity degradation of the TDC 40 are then reduced without compromising TDC resolution.

As discussed in FIG. 1, the error ε[k] includes a time-varying but predictable deterministic part corresponding to (PHR[k]-PHV[k]). Based on the regularly varying deterministic part of the error ε[k], the shift controller 42 dynamically sets the phase offset PHoffset by the shift control signal SEL, such that the phase offset PHoffset is subtracted from the deterministic part of the error ε[k] to become the error ε[k]. For example, when the deterministic part of the error ε[k] is predicted to be in a range of 1/4 (equivalent to a phase of 90 degrees) to 1/2 (180 degrees), the phase offset PHoffset can be set to 90 degrees (equivalent to 1/4), hence the error ε[k] is maintained in a range of 0 to 1/4. Similarly, as time progresses, when the deterministic part of the error ε[k] enters a range of 1/2 to 3/4, the phase offset PHoffset tracks to be set to 180 degrees (1/2 in terms of the period Tv), so the error ε[k] is kept in a range of 0 to 1/2. To compensate the subtracted phase offset PHoffset, the shift controller 42 injects the fractional error correction signal PHF2[k] to the adder 50 to reflect the phase Offset PHoffset; with the fractional error correction signal PHF1[k] indicating the quantized error ε[k], the error ε[k] is obtained by ε[k]=(PHR[k]-PHV[k]+e[k]). In other words, the fractional error correction signals PHF1[k] and PHF2[k] can be analogues to an all-digital phase lock loop (ADPLL). In an embodiment, the variable phase signal PHV[k], an integer, is a fixed point digital word of WI bits. The reference phase signal PHR[k] is a fixed point digital word of (W1+WF) bits combining an integer part of WI bits and a fractional part of WF bits. Each of the fractional error correction signals PHF1[k] and PHF2[k] is a fractional represented by a fixed point digital word of WF bits. The signal PH[ek] is a signed fixed point digital word of (W1+WF) bits including an integer part of WI bits and a fractional part of WF bits.

Please refer to FIG. 5 illustrating an example of the phase shifter 46 according to an embodiment of the invention. In FIG. 5, the phase shifter 46 includes a divider 44 and a phase selector 48. The divider 44 is coupled to the oscillator 10, and arranged to divide the frequency of the variable clock CKV and to provide a plurality of shifted clock candidates CKVp(1), CKVp(2), ... , CKVp(Np) of different phases according to the variable clock CKV. For example, the phase of the shifted clock candidate CKVp(n) is (n-1)*360/Np degrees different from phase of the shifted clock candidate CKVp(1). The phase selector is coupled to the divider 44 and the shift controller 42, and arranged to select one of the shifted clock candidates CKVp(1) to CKVp(Np) as the shifted variable clock CKV' in response to the shift control signal SEL of the shift controller 42.

In an embodiment, the divider 44 is arranged to divide the frequency of the variable clock CKV by two, and to accordingly provide four shifted clock candidates CKVp(1) to CKVp(4) of quadrature phases, with phases of the variable clock CKV and the shifted clock candidate CKVp(n) separated by a phase offset of 90°(n-1) degrees, for n=1 to 4. Please refer to FIG. 6 illustrating the TDC operation based on quadrature phases. With one of the four quadrature phases selected as the shifted variable clock CKV', the full range of the error ε[k] which extends 360 degrees (or one period Tv of the variable clock CKV) is mapped to a smaller range of the error ε[k], which extends only 90 degrees, or a quarter of the period Tv.

For example, when the error ε[k] is predicted to be in a range S0 of 0 to 90 degrees according to the fractional part PHR[k] of the reference phase signal PHR[k], the shift controller 42 selects the shifted clock candidate CKVp(1) as the shifted variable clock, so the error ε[k] is also in a range of 0 to 90 degrees; the shift controller 42 also injects a fractional error correction signal PHF2[k] equivalent to zero degrees to the adder 50. When the error ε[k] is predicted to be in a range S1 of 90 to 180 degrees, the shift controller 42 switches to select the shifted clock candidate CKVp(2) of a 90-degree phase offset as the shifted variable clock CKV', so the error...
The phase shifter 66, e.g., a digital-to-time converter (DTC), is coupled to the frequency reference input 32b and the TDC 40, and arranged to provide a shifted reference clock FREF by delaying (or changing phase of) the frequency reference clock FREF in response to a shift control signal SEL. The variable clock CKV and the shifted reference clock FREF are respectively fed to the TDC 40 as the signals TDC_in and REF_in, so the TDC 40 detects (quantizes) an error $\varepsilon[k]$ (a time difference) between a significant transition of the shifted clock FREF and a prior transition of the variable clock CKV, and provides a fractional error correction signal PHF2[k] in response. In cooperation with the phase shifter 66, the shift controller 62, e.g., a DTC compensator, is coupled to the phase shifter 66 and the adder 50, and arranged to provide the shift control signal SEL (e.g., a DTC digital control) and another fractional error correction shift PHF2[k] in response to the fractional part PHR[k] of the reference phase signal PHR[k]. With support of the shift controller 62 and the phase shifter 66, the TDC range of the TDC 40 is arranged to be less than a fraction of the period $T_v$ of the variable clock CKV.

Please refer to FIG. 8 illustrating cooperation of the phase shifter 66, the shift controller 62, and the TDC 40. While phase lock needs information about the error $\varepsilon[k]$ between a significant transition of the frequency reference clock FREF and a prior significant transition of the variable clock CKV, the shift controller 62 dynamically adjusts the shift control signal SEL and the fractional error correction signal PHF2[k] according to the fractional part of the reference phase signal PHR[k], so the shift control signal SEL and the fractional error correction signal PHF2[k] update following the deterministic part of the error $\varepsilon[k]$. The phase shifter 66 is arranged to change phase (equivalently delay) of the frequency reference clock FREF by a phase offset PHdelay which is set according to the shift control signal SEL, wherein the phase offset PHdelay is such arranged that the error $\varepsilon[k]$ between a significant transition of the shifted reference clock FREF and a subsequent significant transition of the variable clock CKV is less than a fraction of full range of the period $T_v$ (also less than or equal to the error $\varepsilon[k]$). Equivalently, the phase offset PHdelay is subtracted from the error $\varepsilon[k]$ to form the error $\varepsilon[k]$. Because the TDC 40 only quantizes a shorter error $\varepsilon[k]$ instead of the error $\varepsilon[k]$, TDC 40 benefits from a reduced TDC range. The fractional error correction signal PHF2[k] is arranged to compensate the subtracted phase offset PHdelay, as shown in FIG. 7 and FIG. 8.

For example, when the error $\varepsilon[k]$ is in a range of $\frac{1}{4}T_v$, the shift controller 62 sets the phase offset PHdelay to preferably $\frac{(3)}{4}T_v$, then the error $\varepsilon[k]$ to be measured by the TDC 40 is in a range of 0 to $\frac{1}{4}$. When the error $\varepsilon[k]$ is in a range of $\frac{1}{4}$ to $\frac{3}{4}$, the shift controller 62 switches to set the phase offset PHdelay to preferably $\frac{1}{2}T_v$, so the error $\varepsilon[k]$ to be measured by the TDC 40 is maintained in the range of $0$ to $\frac{1}{2}$, rather than full range of 0 to 1. Because the TDC 40 is arranged to respond when a transition of the variable clock CKV and a transition of the shifted reference clock FREF occur in a proximity of the TDC range, and not to respond when transitions of the variable clock CKV and transitions of the shifted reference clock FREF do not occur in a proximity of the TDC range, hardware complexity (e.g., required delay units) of the TDC 40 is effectively reduced, leading to lower power consumption, less supply interference and enhanced linearity, etc.

In an embodiment, frequency of the frequency reference clock FREF is much lower than frequency of the RF variable clock CKV, so the phase shifter 66 only needs to work at low-speed. In an embodiment, the phase shifter 66 is imple-
The variable clock CKV is tracking the frequency reference clock CKR. For generating a variable phase signal PHV[k], a phase accumulator 36 for providing a reference phase signal PHR[k], and a phase shifter 66 (FIG. 7), the phase shifter 76 is coupled to the shift controller 72, and arranged to change phase of the variable clock CKV'. The phase shifter 76 injects the fractional error correction signal PHF2[k] to compensate the phase offset PHO,k, and the reference frequency clock FREF is provided to the power management circuit 74 as the signal REF_in0.

In another embodiment, cooperation of the shift controller 72 and the phase shifter 76 is similar to cooperation of the shift controller 62 and the phase shifter 66 (FIG. 7); the phase shifter 76 delays the frequency reference clock FREF by the phase offset PHo_k in response to the shift control signal SEL, and accordingly provides the shifted variable clock CKV' as the signal TDC_in0. The phase shifter 76 is coupled to the gating signal CON and the signal REF_inO and the REF_in at two inputs, and arranged to provide the signal REF_in by delaying the signals TDC_in0 and REF_in0 are therefore provided according to the variable clock CKV and the frequency reference clock FREF respectively. The power management circuit 74 is coupled to the variable clock input 78a and the frequency reference input 78b for outputting the signals REF_in and TDC_in, wherein the signal TDC_in is provided as a single pulse of the signal TDC_in0 ahead of a subsequent significant transition of the signal REF_in.

In the embodiment of FIG. 3, 5 and FIG. 7, the oscillator 10 works as a tuned oscillator; it is tuned so the variable clock CKV is tracking the frequency reference clock FREF. The signal PHE[k] provided by the adder 50 feeds back to the oscillator 10 through the loop filter 38, and then the variable clock CKV can be further tuned in a finer sense. In an embodiment, the loop filter 38 is a digital low pass filter. The loop filter 38 can be constructed as a combination of FIR (finite impulse response) and IIR (infinite impulse response) filters. For example, in an embodiment, the loop filter 38 is arranged to provide the OTW by linearly combining the signal PHE and an accumulation of the signal PHE, so the frequency synthesizer is a type II loop.

In the embodiment shown in FIG. 3, 5 and FIG. 7, the TDC 40 receives the high-speed shifted variable clock CKV' (FIG. 3 and FIG. 5) or the variable clock CKV (FIG. 7) as the signal TDC_in, and receives the low-speed frequency reference clock FREF (FIG. 3 and FIG. 5) or the shifted reference clock FREF' (FIG. 7) as the signal REF_in. The TDC 40 quantizes the time difference between the signals TDC_in and REF_in, and updates the fractional error correction signal PHF2[k] at significant transitions of the reference phase signal PHR[k]. However, the TDC 40 is kept receiving the high-speed toggling signal TDC_in, no matter the fractional error correction signal PHF2[k] of the TDC 40 is triggered to update or not. High-speed toggling consumes large power, induces serious supply interference, and therefore degrades linearity of time-to-digital conversion. To address the issue, a power management is arranged to suppress unnecessary pulses in the signal TDC_in, only to keep a single pulse closest to a subsequent significant transition of the signal REF_in, such that power consumption and supply interference are reduced without comprising normal time-to-digital conversion.

Please refer to FIG. 9 illustrating a frequency synthesizer 70 according to an embodiment of the invention. Similar to the frequency synthesizers 30 and 60, the frequency synthesizer 70 includes an FCW input 32a for receiving an FCW, a frequency reference input 32b for receiving a frequency reference clock FREF, an oscillator 10 for generating a variable clock CKV, a re-timer 12 for providing a re-timed reference clock CKR by re-timing the frequency reference clock FREF at significant transition of the variable clock CKV, a reference phase accumulator 34 for providing a reference phase signal PHR[k] by accumulating the FCW in response to the re-timed reference clock CKR, a variable phase accumulator 36 for providing a variable phase signal PHV[k] by accumulating unit count at significant transitions of the variable clock CKV, a TDC 80 for providing a fractional error correction signal PHF2[k] by quantizing a time difference between the signals TDC_in and REF_in, an adder 50 for providing the signal PHE[k], and a loop filter 38 for providing an OTW to the oscillator 10 in response to the signal PHE[k].

In addition, the frequency synthesizer 70 further includes a variable clock input 78a for receiving a signal TDC_in0, another frequency reference input 78b for receiving a signal REF_in0, a shift controller 72, a phase shifter 76 and a power management circuit 74. The shift controller 72 is arranged to provide another fractional error correction signal PHF2[k] and the shift control signal SEL in response to a fractional part PHF2[k] of the reference phase signal PHR[k], so the adder 50 produces the signal PHE by adding an arithmetic difference (PHR[k]-PHV[k]) and an arithmetic sum (PHF1[k]+PHF2[k]). The phase shifter 76 is coupled to the shift controller 72, and arranged to change phase of the variable clock CKV or the frequency reference clock FREF, and the signals TDC_in0 and REF_in0 are therefore provided according to the variable clock CKV and the frequency reference clock FREF respectively. The power management circuit 74 is coupled to the variable clock input 78a and the frequency reference input 78b for outputting the signals REF_in and TDC_in, wherein the signal TDC_in is provided as a single pulse of the signal TDC_in0 ahead of a subsequent significant transition of the signal REF_in.

In an embodiment, cooperation of the shift controller 72 and the phase shifter 76 is similar to cooperation of the shift controller 42 and the phase shifter 46 (FIG. 3); the phase shifter 76 changes phase of the variable clock CKV by the phase offset PHo_k in response to the shift control signal SEL, and accordingly provides the shifted variable clock CKV' as the signal TDC_in0. The phase shifter 76 injects the fractional error correction signal PHF2[k] to compensate the phase offset PHO,k, and the variable clock CKV is provided to the power management circuit 74 as the signal TDC_in0. Through cooperation of the shift controller 72 and the phase shifter 76, the time difference (the error -e[k]) between the signals TDC_in0 and REF_in0 is kept in a range shorter than full range of the period T_v.

Please refer to FIG. 10 illustrating a power management circuit 74A according to an embodiment of the invention, which can be adopted to implement the power management circuit 74 shown in FIG. 9. The power management circuit 74A includes two logic gates 82a and 82b, and a delay (delay element) 82c. The logic gate 82a is coupled to the signal REF_in0 and the REF_in at two inputs, and arranged to provide a gating signal CON in response to a logic operation result of the signals REF_in0 and REF_in, e.g., an AND of the signal REF_in0 and an inversion of the signal REF_in. The delay gate 82c is coupled to the signal REF_in0 and the logic gate 82a, and arranged to provide the signal REF_in by delaying the signal REF_in0 with a delay time Tdelay. The logic gate 82b is coupled to the gating signal CON and the signal TDC_in0 at two inputs, and arranged to provide the signal TDC_in in response to an AND logic operation result of the signal TDC_in0 and the gating signal CON.

When the signal REF_in0 transits from logic 0 to logic 1 at a significant transition 84a, the logic gate 82a is arranged to set the gating signal to logic 1, and when the signal REF_in transits from logic 0 to logic 1 at a significant transition 84b, the logic gate 82a is arranged to set the gating signal CON back to logic 0. Hence, the gating signal CON maintains a window of logic 1 during the delay time T_delay between the significant transitions 84a and 84b. When the gating signal CON is of logic 0, the logic gate 82b is arranged to suppress pulses of the signal TDC_in0, and when the gating signal...
CON is of logic 1, the logic gate 82b is arranged to provide a single pulse 86a ahead of the subsequent significant transition 84b for the signal TDC_in by tracking the signal TDC_in0. In other words, as the signal TDC_in is provided according to the signal TDC_in0, only the single pulse 86a is reserved in the signal TDC_in, and other unnecessary pulses of the signal TDC_in0, such as pulses 865 and 86c, are suppressed by the gating signal CON. The signals REF_in and TDC_in are transmitted to the TDC 80, so the error –e[k] is obtained as the TDC 80 detects (quantizes) a timing difference corresponding to an interval THA between a significant transition 84c of the pulse 86a and the subsequent significant transition of the signal REF_in.

By suppressing unnecessary pulses and maintaining a single pulse before a subsequent significant transition of the signal REF_in, high-speed toggling of the TDC 80 is avoided without compromising normal function of the TDC 80, thus power consumption is effectively reduced, and linearity of time-to-digital conversion is enhanced due to suppressed supply interference. The proper operation of the TDC 80 is not violated whether one (or more) pulse, such as the pulse 86a, appears in the signal TDC_in after the significant transition 84b of the signal REF_in, since the interval THA is measured (updated) before the significant transition 86d. The extra pulses, however, could negatively affect the power supply network operation, hence they are not desirable.

Due to cooperation of the shift controller 72 and the phase shifter 76, duration of the error –e[k] between the signals TDC_in0 and REF_in0 is in the TDC range shorter than the period Tv, and the delay time Tdelay can be set shorter than the period Tv. On the contrary, if duration of the error –e[k] is long. However, as the delay time Tdelay is longer than the period Tv, the window tends to capture more than one pulse in the signal TDC_in, and linearity of time-to-digital conversion could be, therefore, degraded, since more than one pulse before the significant transition 84b induce higher supply interference when the interval THA is measured.

For a proper setting of the delay time Tdelay, a lower bound of the delay time Tdelay is the TDC range, an upper bound is set to avoid additional pulse(s) before the significant transition 84b. Accordingly, an accepted variation of the delay time Tdelay is plus or minus (Tv/2–Tc)/2, where Tc denotes the TDC range.

Please refer to FIG. 11 and FIG. 12; FIG. 11 illustrates another power management circuit 74b according to an embodiment of the invention, and FIG. 12 demonstrates operation of the power management circuit 74b in two different cases. The power management circuit 74b can be adopted to implement the power management circuit 74 shown in FIG. 9. The power management circuit 74b includes two logic gates 82a and 82b, a delay line 82c, and a level sense circuit 82d. The logic gate 82a is coupled to the signal REF_in0 and the REF_in at two inputs, and arranged to provide a gating signal CON in response to a logic operation result of the signals REF_in0 and REF_in. The delay line 82c is coupled to the signals REF_in and the logic gate 82a, and arranged to provide the signal REF_in0 with a delay time Tdelay. The level sense circuit 82d is coupled to the signal TDC_in0 and the gating signal CON at two inputs, and arranged to provide another gating signal CON' in response to the signal TDC_in0 and the gating signal CON. The logic gate 82d is coupled to the gating signal CON' and the signal TDC_in0 at two inputs, and arranged to provide the signal TDC_in in response to an AND logic operation result of the signal TDC_in0 and the gating signal CON.

As shown in FIG. 12, when the REF_in0 transits from logic 0 to logic 1 at a significant transition 84a, the logic gate 82a is arranged to set the gating signal CON to logic 1, and when the signal REF_in transits from logic 0 to logic 1 at a significant transition 84b, the logic gate 82a is arranged to set the gating signal CON back to logic 0. As shown in case 1 of FIG. 12, when the gating signal CON transits from logic 0 to logic 1 at a transition 90a, if the signal TDC_in0 is of logic 0, the level sense circuit 82d is arranged to set the gating signal CON' to logic 1 at a transition 90b. On the other hand, as shown in case 2 of FIG. 12, when the gating signal CON transits from logic 0 to logic 1 at the transition 90a, if the signal TDC_in0 is of logic 1, the level sense circuit 82d is arranged to set the gating signal CON' back to logic 0 when the gating signal CON transits back to logic 0. The level sense circuit 82d is further arranged to set the gating signal CON' back to logic 0 when the gating signal CON transits back to logic 0. In other words, during the window of the delay time Tdelay opened by the gating signal CON, the level sense circuit 82d opens a second window in the gating signal CON', when the signal TDC_in0 is of logic 0.

When the gating signal CON' is of logic 0, the logic gate 82b is arranged to suppress pulses of the signal TDC_in0, like the pulses 88a and 88b. When the gating signal CON' is of logic 1, the logic gate 82b is arranged to provide a single pulse 86a for the signal TDC_in by tracking the signal TDC_in0, such that only a significant transition 84b of the pulse 86a exists ahead of the significant transition 84b of the signal REF_in. The TDC 80 detects the error –e[k] by measuring an interval between the significant transitions 84a and 84b. In the signal TDC_in, because only the single pulse 86a presents before the significant transition 84b, unnecessary toggling of the TDC 80 is prevented, and linearity of the TDC 80 is enhanced.

As shown in case 2 of FIG. 12, if the gating signal CON is used to gate pulses of the signal TDC_in0, an additional pulse between the significant transition 90a and a falling edge 90d would be included in the signal TDC_in, and it could degrade linearity of the TDC 80. However, because the level sense circuit 82d adaptively avoids the duration when the signal TDC_in0 is of logic 1, the additional pulse is excluded by the narrower window of the gating signal CON; thus, existence of only a single pulse before the significant transition 84b is ensured for linearity preservation. By operation of the level sense circuit 82d, the power management circuit 74b is more robust with improved immunity against delay variation of the delay line 82c, since tolerable delay variation of the delay time Tdelay is expanded to plus or minus (Tv–Tc)/2.

Please refer to FIG. 13 illustrating an example of the level sense circuit 82d, which includes an SR latch formed by two NAND gates 92a and 92b, as well as an inverter 94. The NAND gate 92a is respectively coupled to the signal TDC_in0, a node n0 and a node n1 at two inputs and an output. The NAND gate 92a is respectively coupled to the gating signal CON, the node n1 and the node n0 at two inputs and an output. The inverter 94 is coupled between the NAND gate 92b and the logic gate 82d. The gating signal CON is latched at logic 0 when the signal TDC_in0 is of logic 1, and released to follow the gating signal CON when the signal TDC_in0 is of logic 0.

To sum up, supporting peripherals for TDC in digital frequency synthesizer are provided. While monitoring the time difference (phase error) between the variable clock and the frequency reference clock by the TDC, phase of one of the
variable clock and the frequency reference clock is adaptively
shifted according to accumulation of the FCW, so the time
difference is maintained in a partial range of the period of
the variable clock, and TDC range can thus be set less than the
period of the variable clock. In addition, unnecessary high-
frequency toggling pulses to the TDC can be gated without
compromising normal function of the TDC. Shorter TDC
range and gated TDC toggling lead to advantages such as
enhanced linearity of time-to-digital conversion, reduced
hardware complexity, lower power consumption, smaller lay-
out area, less required decoupling capacitance, and sup-
pressed supply interference of the frequency synthesizer.

While the invention has been described in terms of what is
presently considered to be the most practical and preferred
embodiments, it is to be understood that the invention needs
not be limited to the disclosed embodiment. On the contrary,
it is intended to cover various modifications and similar
arrangements included within the spirit and scope of the
appended claims which are to be accorded with the broadest
interpretation so as to encompass all such modifications and
similar structures.

What is claimed is:

1. A time-to-digital system comprising:
   a frequency reference input for receiving a frequency ref-
   erence clock;
   a variable clock input for receiving a variable clock, said
   variable clock being of substantially higher frequency
   than said frequency reference clock;
   a power management circuit coupled to said frequency
   reference input and said variable clock input, said power
   management circuit outputting a delayed frequency ref-
   erence clock and a single pulse of said variable clock
   ahead of a transition of said delayed frequency reference
   clock, wherein a second pulse transition of said single
   pulse occurs at said transition of said delayed frequency
   reference clock;
   a time-to-digital converter (TDC) for producing a digital
   TDC output by quantizing a time difference between a
   first pulse transition of said single pulse and said transi-
   tion of said delayed reference clock, said TDC coupled
to said power management circuit.

2. The time-to-digital system of claim 1, wherein said
   power management circuit comprises:
   a first logic gate coupled to said frequency reference clock
   and said delayed frequency reference clock, and
   arranged to provide a gating signal in response to a first
   logic operation result of said frequency reference clock
   and said delayed frequency reference clock;
   a delayer coupled to said frequency reference clock for
   providing said delayed frequency reference clock by
   delaying said frequency reference clock; and
   a second logic gate coupled to said gating signal and said
   variable clock for providing said single pulse of said
   variable clock in response to a second logic operation
   result of said variable clock and said gating signal.

3. The time-to-digital system of claim 2, wherein when said
   frequency reference clock transits from a first level to a sec-
   ond level, said first logic gate is arranged to set said gat-
   ing signal to said first level; and wherein when said
gating signal is of said first level, said level sense circuit
   is further arranged to set said second gating signal to said
   second level while said variable clock is of said first level,
   and when said gating signal is of said second level, said
   second logic gate is arranged to provide said single pulse of
   said variable clock by tracking said variable clock.

4. The time-to-digital system of claim 1, wherein said
   power management circuit comprises:
   a first logic gate coupled to said frequency reference clock
   and said delayed frequency reference clock, and
   arranged to provide a first gating signal in response to a
   first logic operation result of said frequency reference clock
   and said delayed frequency reference clock;
   a delayer coupled to said frequency reference clock for
   providing said delayed frequency reference clock by
   delaying said frequency reference clock;
   a level sense circuit coupled to said variable clock, said first
   gating signal and said second logic gate for providing a
   second gating signal in response to said variable clock
   and said first gating signal;
   a second logic gate coupled to said second gating signal
   and said variable clock for providing said single pulse of
   said variable clock in response to a second logic operation
   result of said variable clock and said second gating
   signal.

5. The time-to-digital system of claim 4, wherein when said
   frequency reference clock transits from a first level to a sec-
   ond level, said first logic gate is arranged to set said first
gating signal to said second level, and when said delayed frequency
reference clock transits from said first level to said second
level, said first logic gate is arranged to set said first gating
signal to said first level; and wherein when said first gating
signal transits from said first level to said second level while
said variable clock is of said first level, said level sense circuit
is arranged to set said second gating signal to said second
level; and when said first gating signal transits from said first
level to said second level while said variable clock is of said
second level, said level sense circuit is arranged to set said
second gating signal to said second level when said variable
clock transits back to said first level.

6. The time-to-digital system of claim 5, wherein when said
   second gating signal is of said first level, said second logic
   gate is arranged to suppress pulses of said variable clock;
   and when said second gating signal is of said second level,
   said second logic gate is arranged to provide said single pulse of
   said variable clock by tracking said variable clock.

7. The time-to-digital system of claim 6, wherein said level
   sense circuit is further arranged to set said second gating
   signal to said first level when said first gating signal transits to
   said first level.

8. The time-to-digital system of claim 4, wherein said level
   sense circuit comprises a latch.

9. The time-to-digital system of claim 1 further comprising:
   a phase shifter coupled to said power management circuit,
   and arranged to adjust a second time difference between
   a transition of said frequency reference clock and a
   transition of said variable clock, such that said second
   time difference is less than a period of said variable
   clock.

10. The time-to-digital system of claim 1 further comprising:
    an oscillator coupled to said variable clock input for tuning
    periods of said variable clock according to said digital
    TDC output, such that said time-to-digital system func-
    tions as a frequency synthesizer.

11. A frequency synthesizer comprising:
    a power management circuit arranged to output a second
    reference clock and a second variable clock in response
to a first reference clock and a first variable clock, such
    that a single pulse between a transition of said first
    reference clock and a subsequent transition of said sec-
    ond reference clock is provided in said second variable
    clock.
19. The frequency synthesizer of claim 11 further comprising:

- a level sense circuit coupled to said first variable clock, said level sense circuit is arranged to set said second gating signal in response to a first logic operation result of said first reference clock and said second reference clock;

- a second logic gate coupled to said gating signal and said first variable clock for providing said second variable clock;

- a second logic gate coupled to said second gating signal in response to said first logic operation result of said first reference clock and said second reference clock;

- a delay gate coupled to said first reference clock and said first logic gate for providing said second reference clock by delaying said first reference clock;

- a level sense circuit coupled to said first variable clock, said first gating signal and said second logic gate for providing said second variable clock by delaying said first reference clock;

- a second logic gate coupled to said second variable clock and said second logic gate for providing said second variable clock by delaying said first variable clock.

20. The frequency synthesizer of claim 19, wherein when said first reference clock transits from a first level to a second level, said first logic gate is arranged to set said gating signal to said second level, and when said second reference clock transits from said first level to said second level, said first logic gate is arranged to set said gating signal to said first level and when said second reference clock is of said first level, said second logic gate is arranged to suppress pulses of said second variable clock; and when said gating signal is of said second level, said second logic gate is arranged to provide said single pulse of said second variable clock by tracking said first variable clock.
22. A time-to-digital system comprising:
a frequency reference input for receiving a frequency reference clock;
a variable clock input for receiving a variable clock, said variable clock being of substantially higher frequency than said frequency reference clock;
a power management circuit coupled to said frequency reference input and said variable clock input, said power management circuit outputting a delayed frequency reference clock and only one single pulse of said variable clock ahead of a transition of said delayed frequency reference clock;
a time-to-digital converter (TDC) for producing a digital TDC output, said TDC coupled to said power management circuit.

23. A time-to-digital system comprising:
a frequency reference input for receiving a frequency reference clock;