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Tohidian et al.

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(54) **QUADRATURE LC TANK DIGITALLY CONTROLLED RING OSCILLATOR**

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H03K 5/133 (2014.01)
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CPC *H03K 5/133* (2013.01); *H03B 5/124* (2013.01); *H03B 5/1212* (2013.01);
(Continued)

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CPC H03K 3/0315; H03K 3/0322; H03K 5/133; H03K 3/011; H03B 5/1228;
(Continued)

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(57) **ABSTRACT**

A quadrature LC tank based digitally controlled ring oscillator (DCO). The oscillator structure incorporates a plurality of stages, each stage including a buffer and a series LC tank. Four stages are coupled together to create a 360 degree phase shift around a loop. The oscillation frequency of the oscillator is the same as the resonant frequency of each LC tank, therefore it avoids quality factor degradation of LC tanks found in the prior art. In one example embodiment, class-D amplifiers are used to drive each of the LC tanks. Capacitor banks before at the input and output of the buffers provide coarse and fine tuning of the frequency of oscillation. The high efficiency exhibited by these amplifiers results in very good phase noise performance of this oscillator. The oscillator utilizes a startup circuit to launch oscillation upon power on.

29 Claims, 25 Drawing Sheets
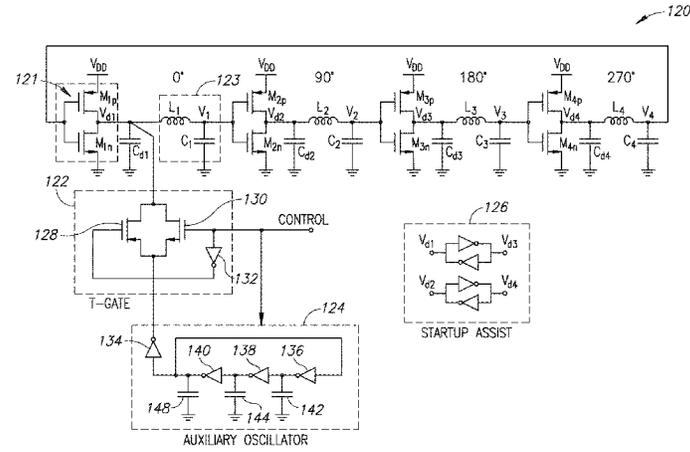
(51) **Int. Cl.**
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   H03B 5/12   (2006.01)
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10

OSCILLATOR A

OSCILLATOR B

M1A   M2A

M3A

M4A

CROSSED CONNECTION

DIRECT CONNECTION

FIG.1

PRIOR ART

DIRECT CONNECTION

CROSS CONNECTION

V_{I+}

V_{CON}

V_{O-} V_{O+}

V_{I+} M3 M1   M2 M4 V_{I-}

V_{I-}

OSCILLATOR 1

V_{O-}

V_{O+}

$\pi + (n-1)\pi/n$

$(n-1)\pi$

V_{I+} V_{O-}

V_{I-} V_{O+}

OSCILLATOR 2

$\pi + 2\pi/n$

$2\pi/n$

V_{I+} V_{O-}

V_{I-} V_{O+}

OSCILLATOR N−1

$\pi + \pi/n$

π/n

V_{I+} V_{O-} 0

V_{I-} V_{O+} π

OSCILLATOR N

20
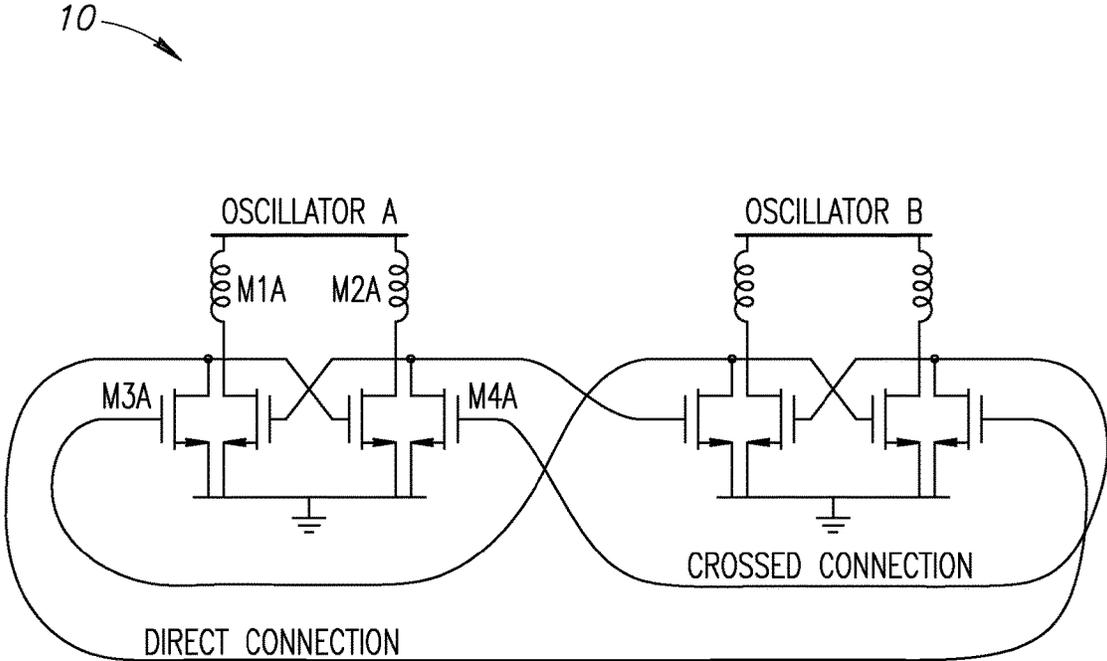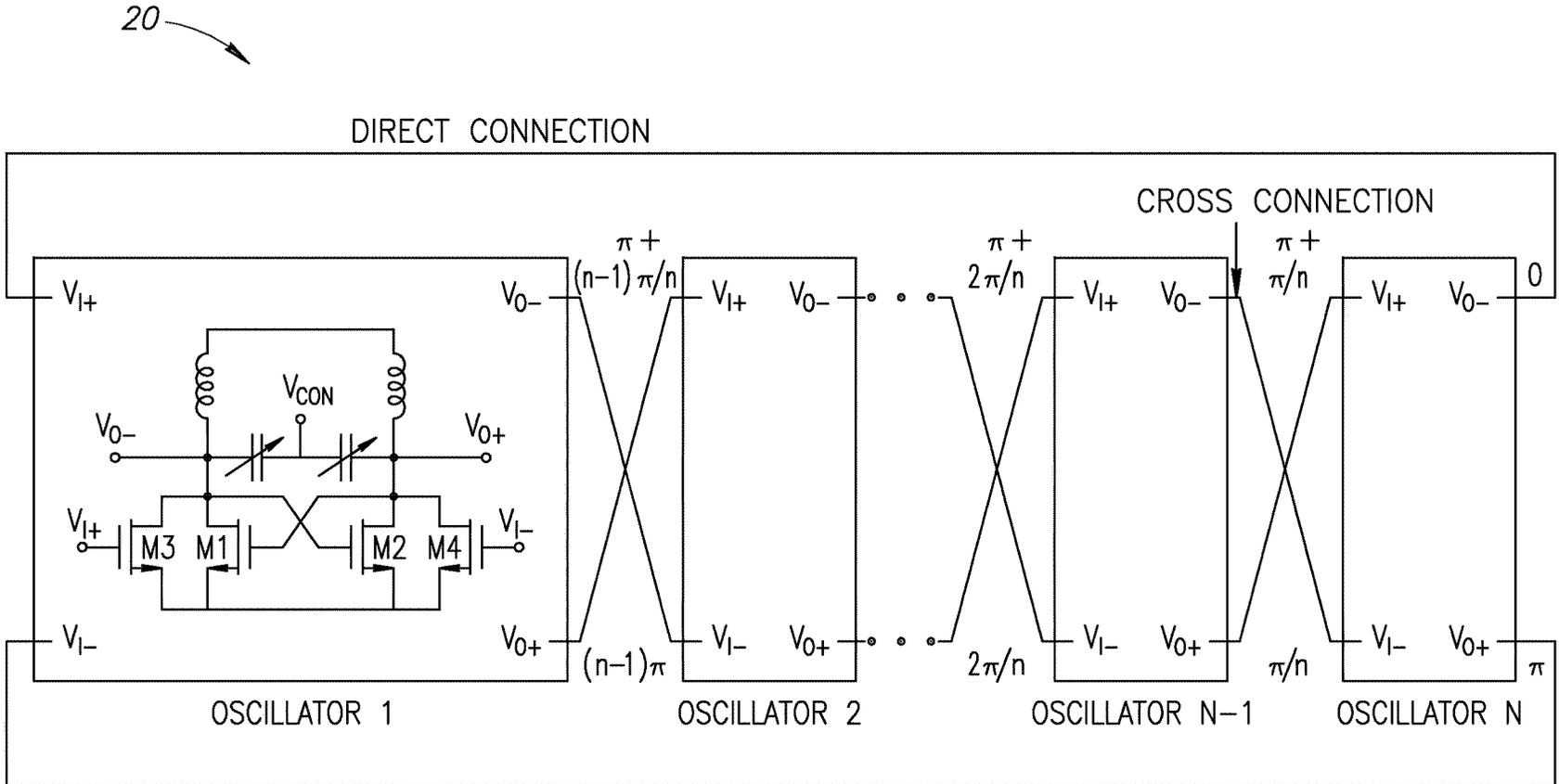
FIG.2

PRIOR ART

30
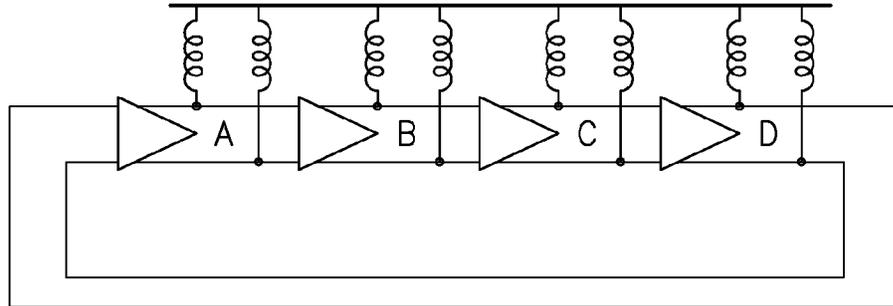
FIG.3A
PRIOR ART

40
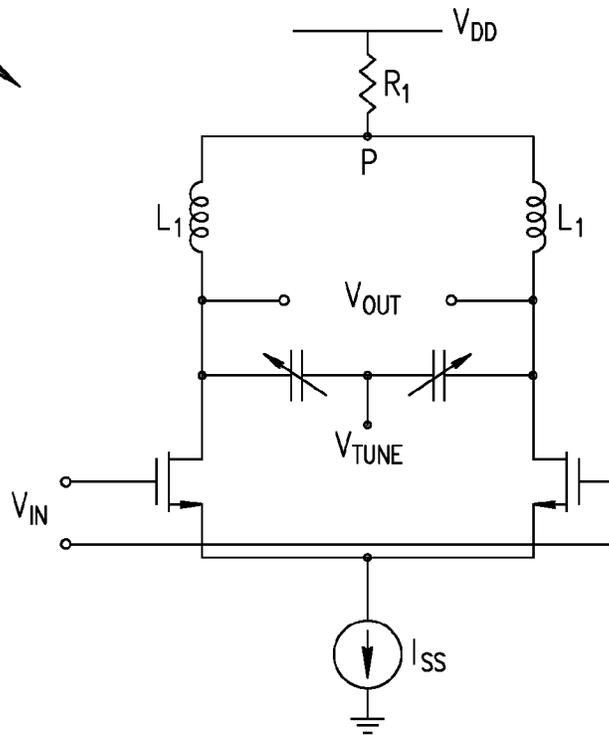
FIG.3B
PRIOR ART

50
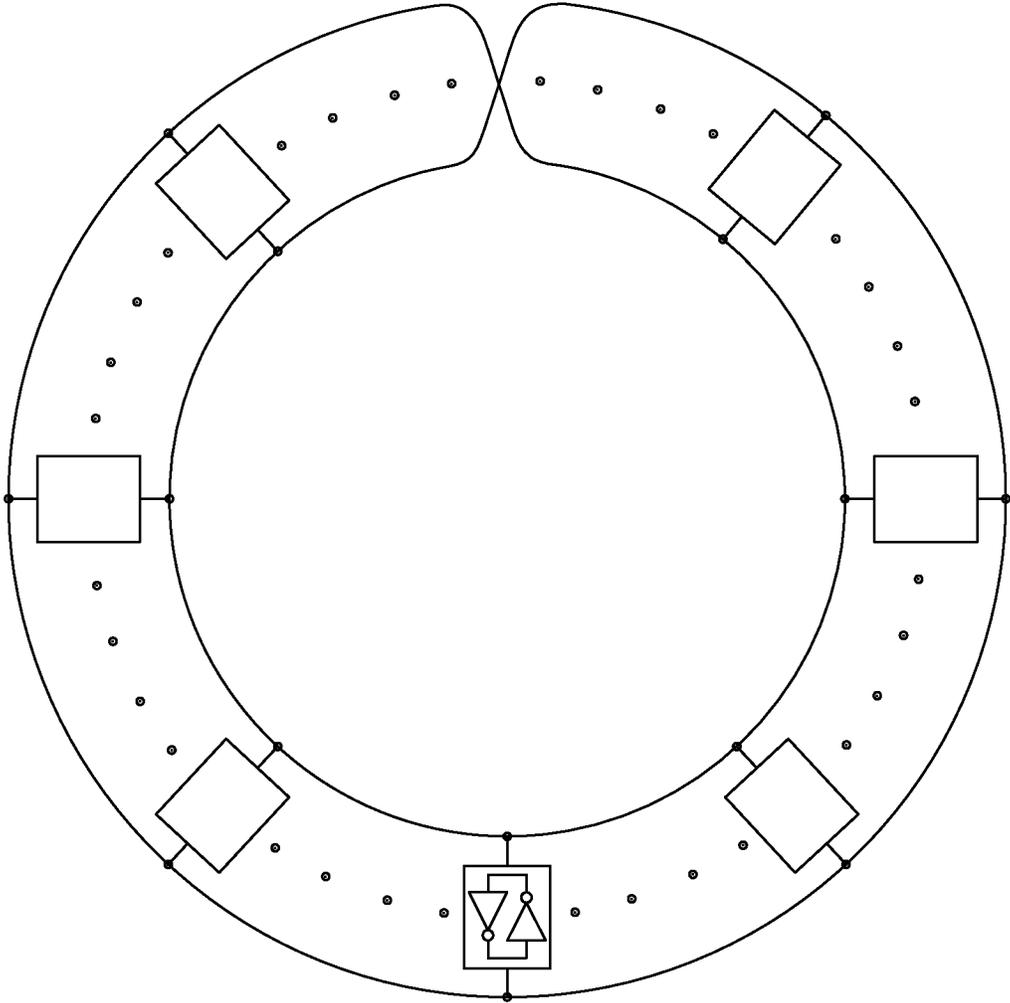
FIG.4
PRIOR ART

FIG.5A
PRIOR ART

70
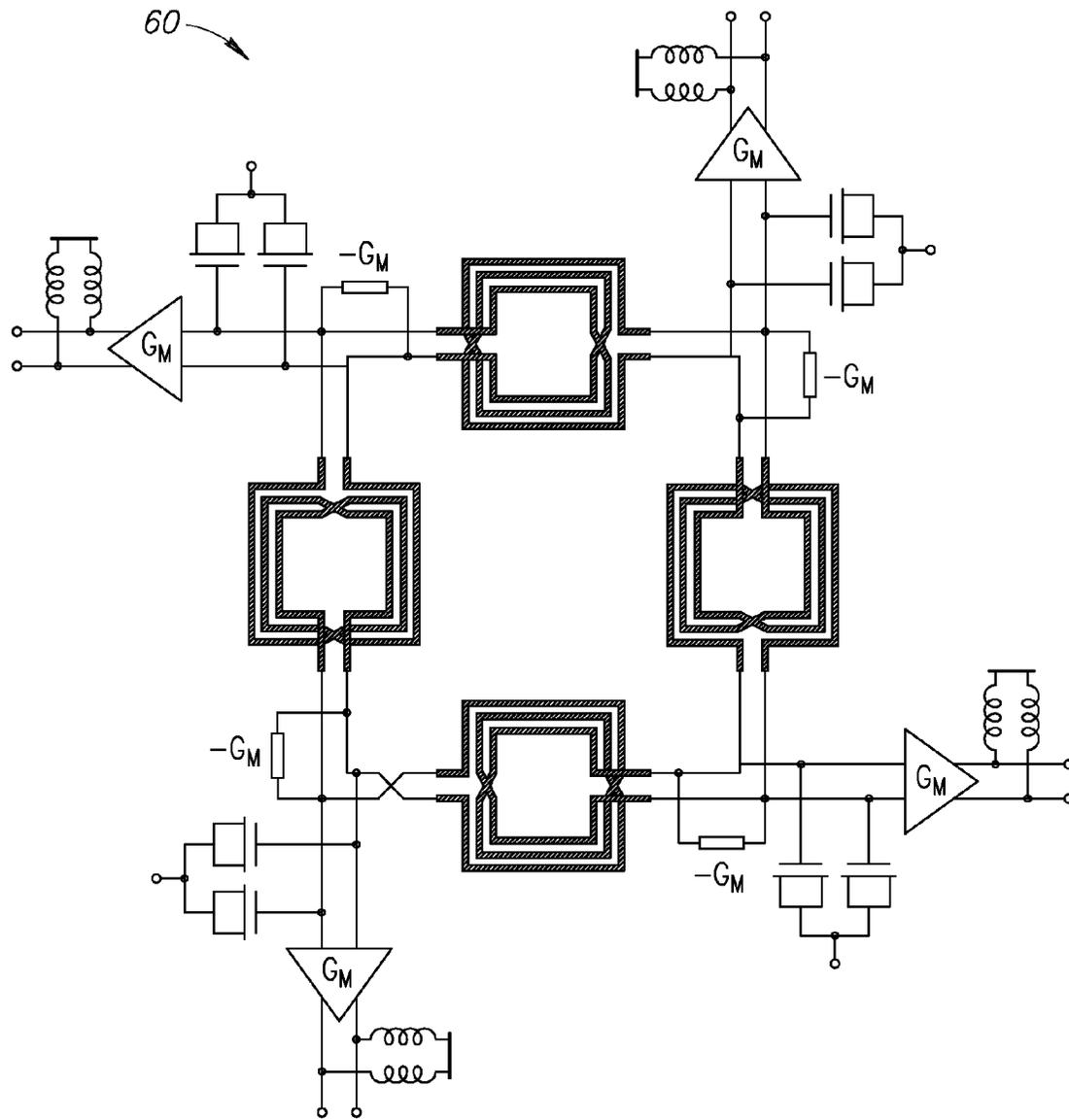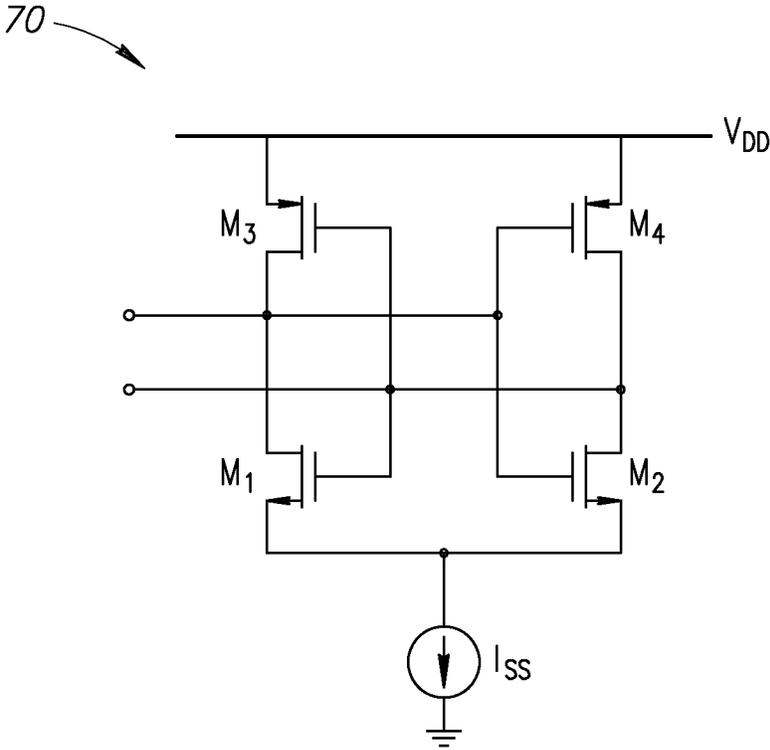
FIG.5B
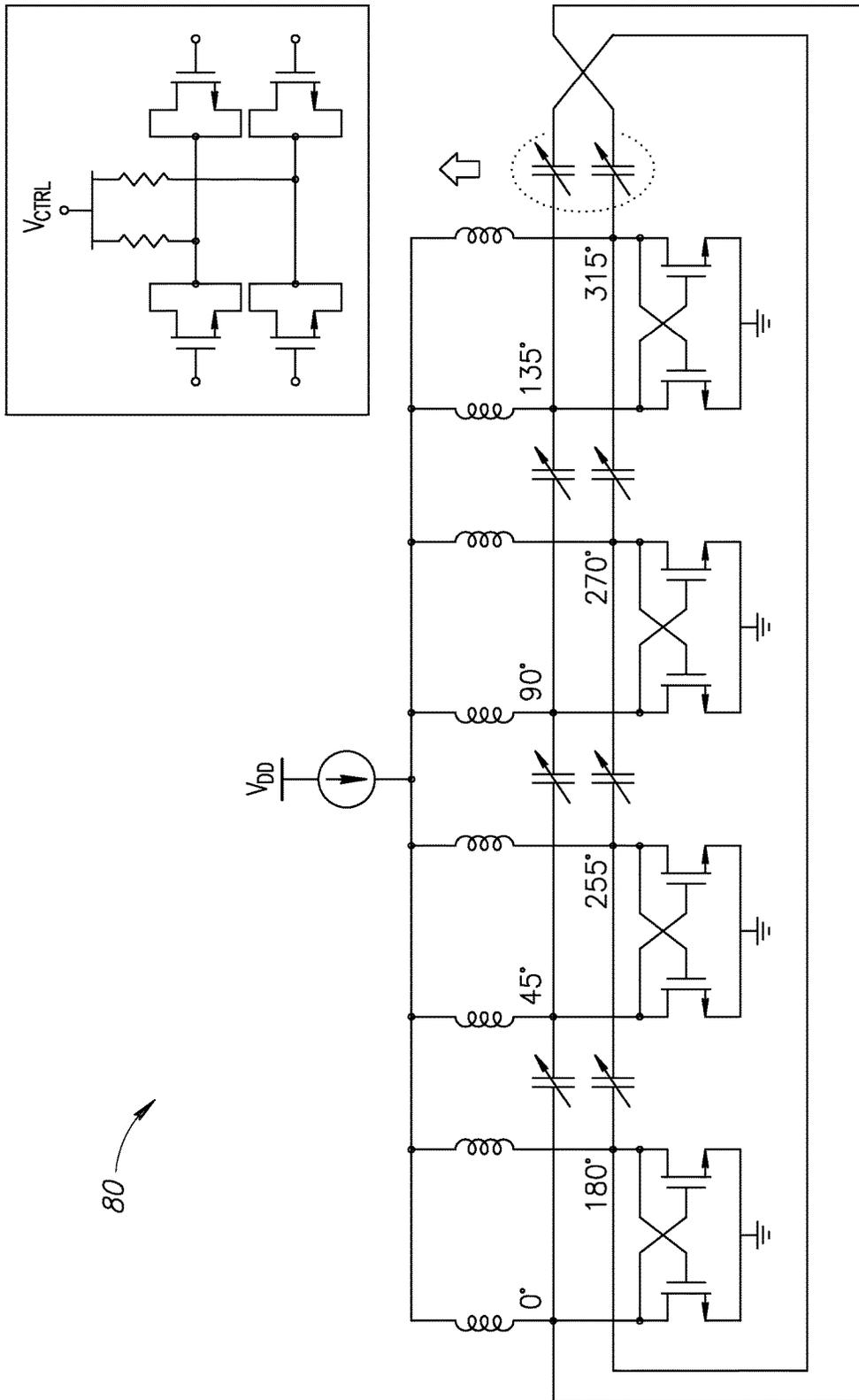
PRIOR ART

FIG.6
PRIOR ART
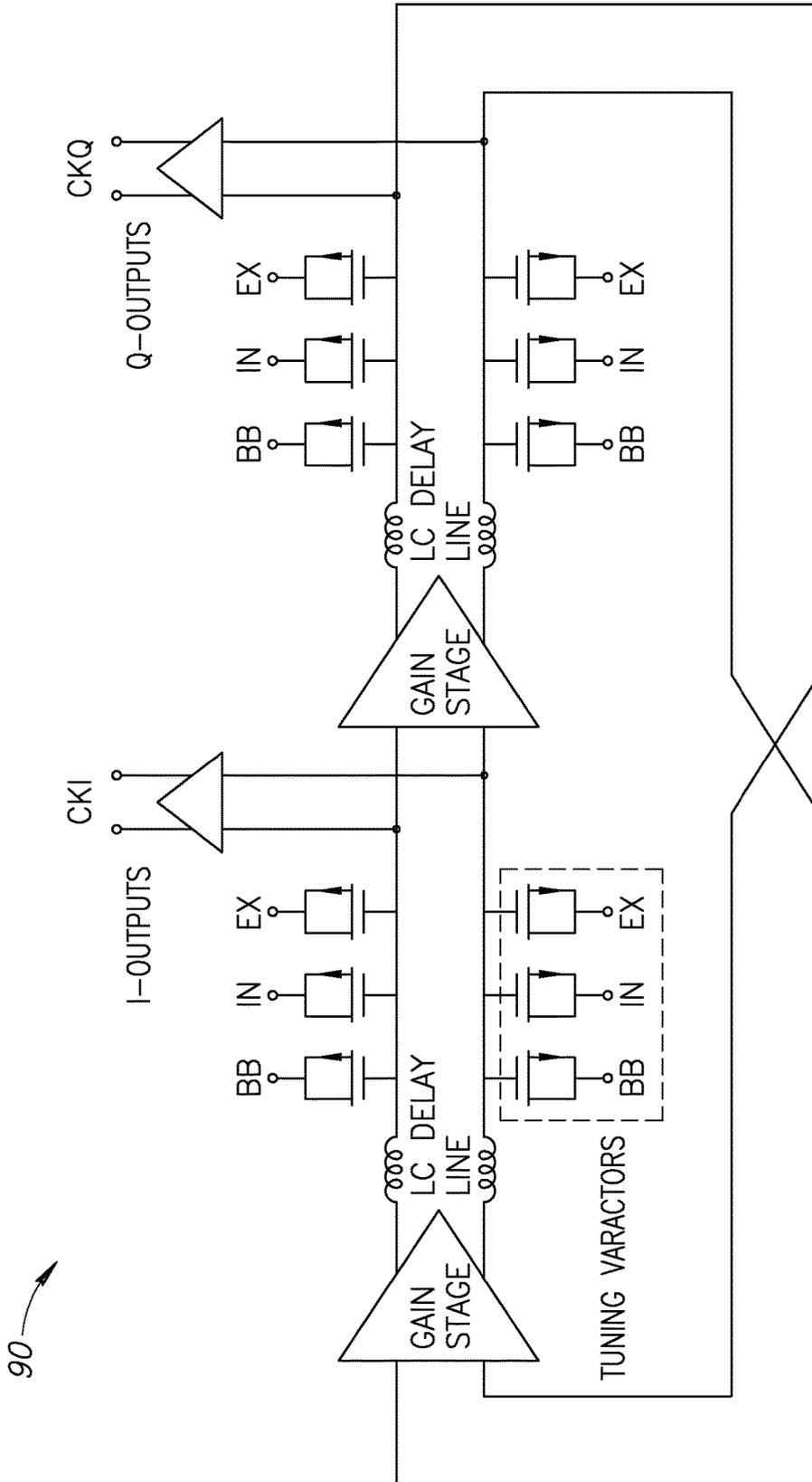
FIG.7A
PRIOR ART

100
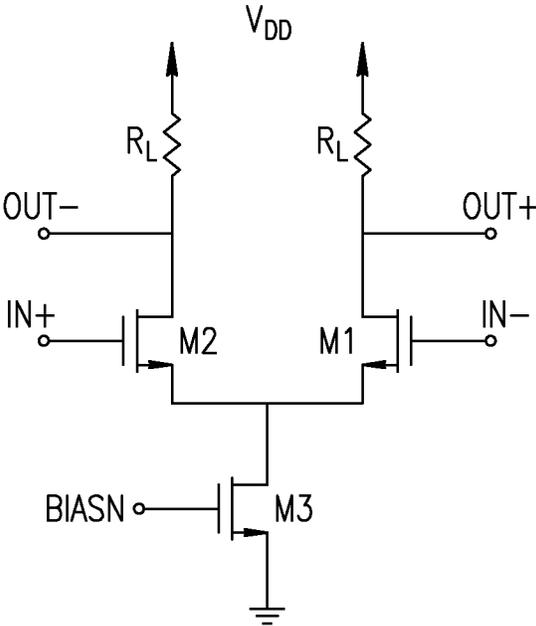
FIG.7B

PRIOR ART

FIG.8A

FIG.8B

$$f= \frac{1}{2\pi\sqrt{LC}}$$

MAG=Q

112

FIG.8C

PHASE=−90°

$$f= \frac{1}{2\pi\sqrt{LC}}$$

114
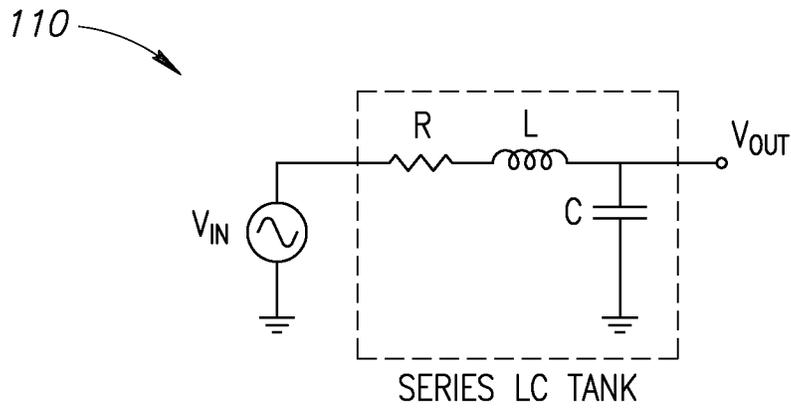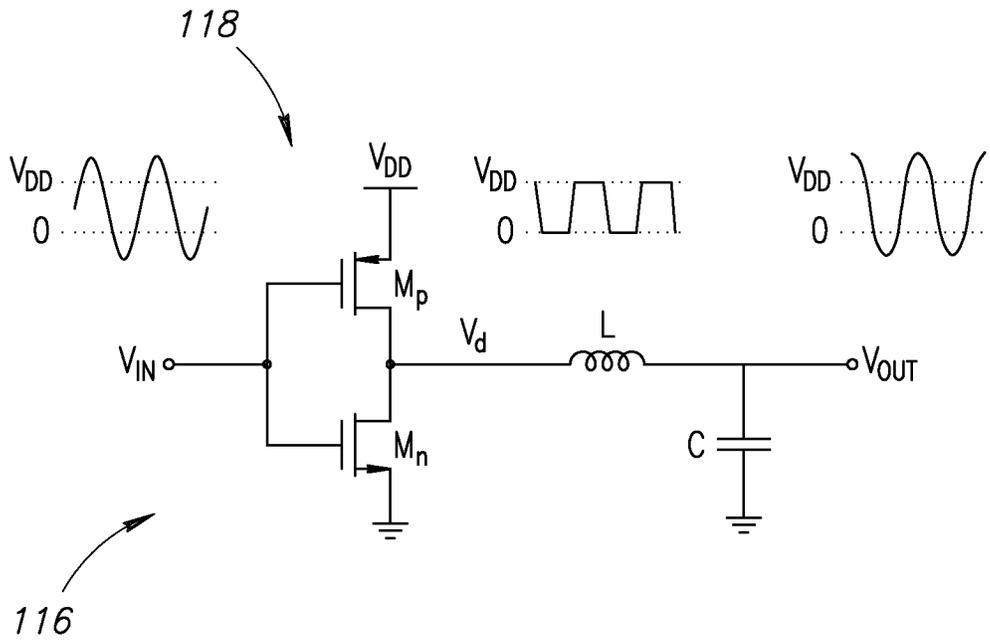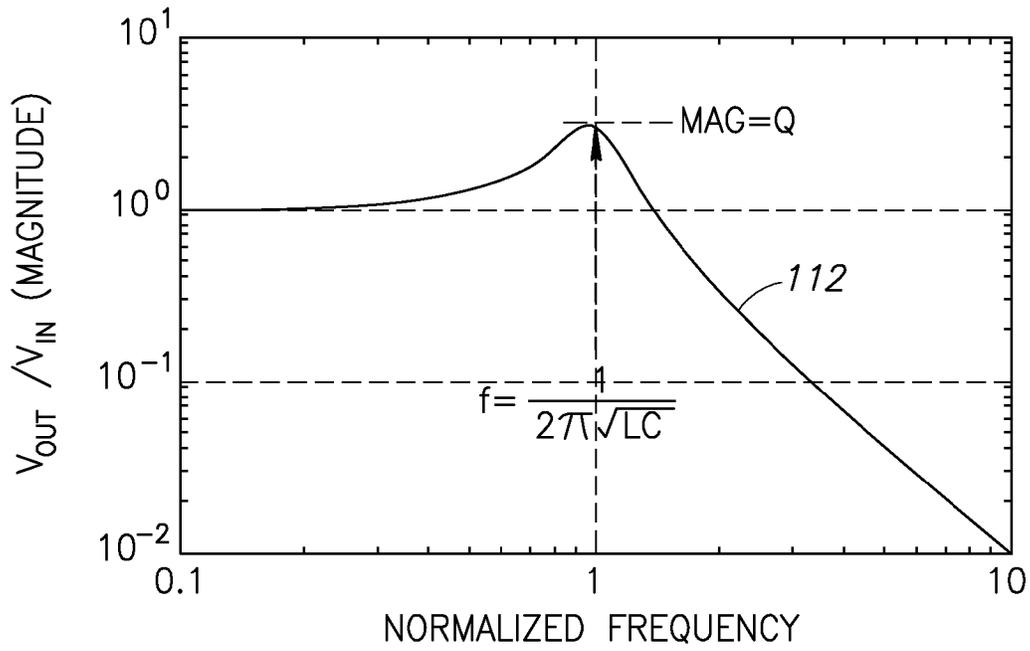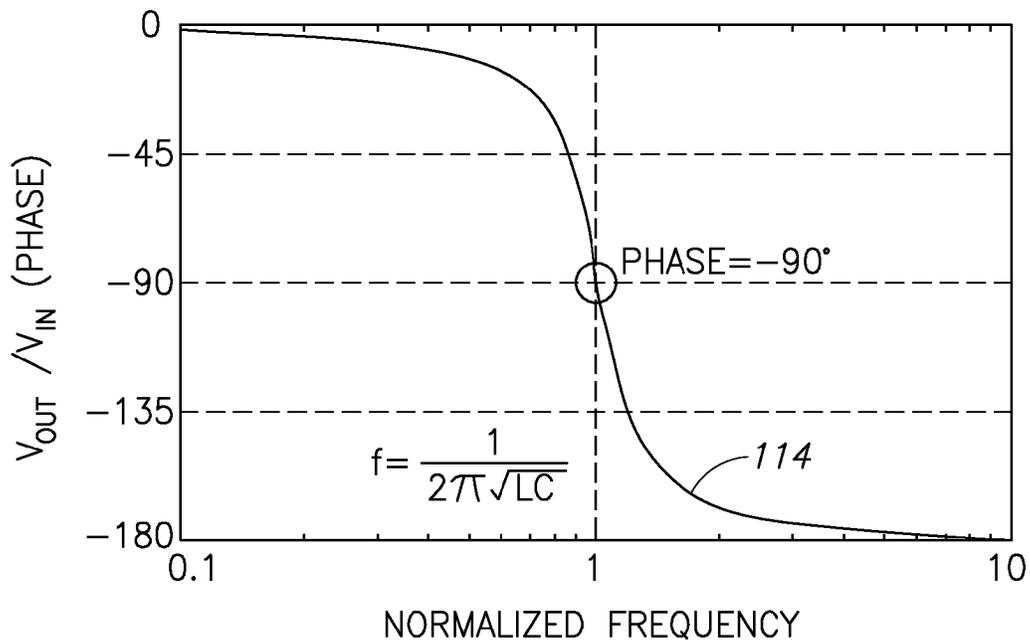
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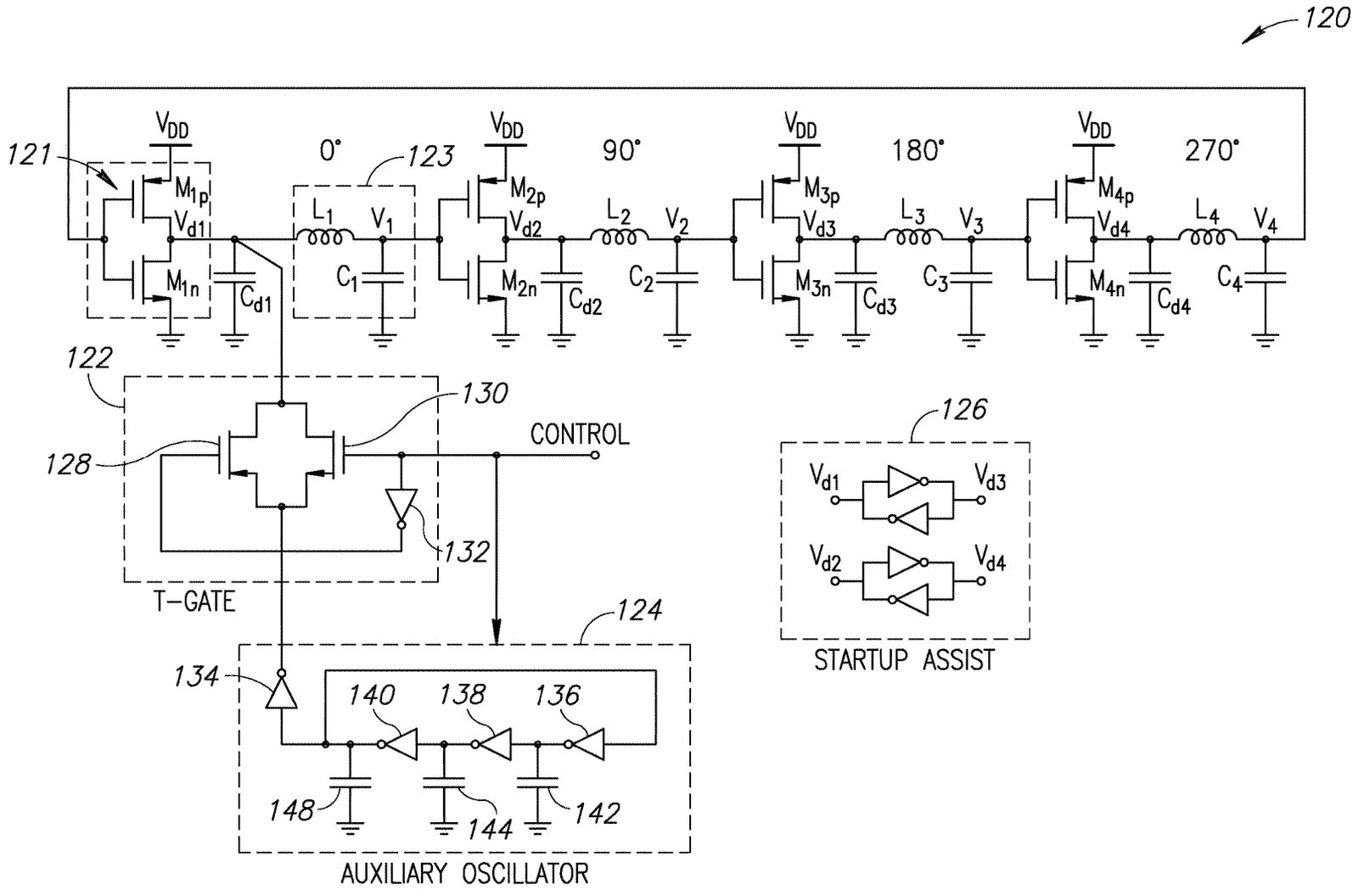
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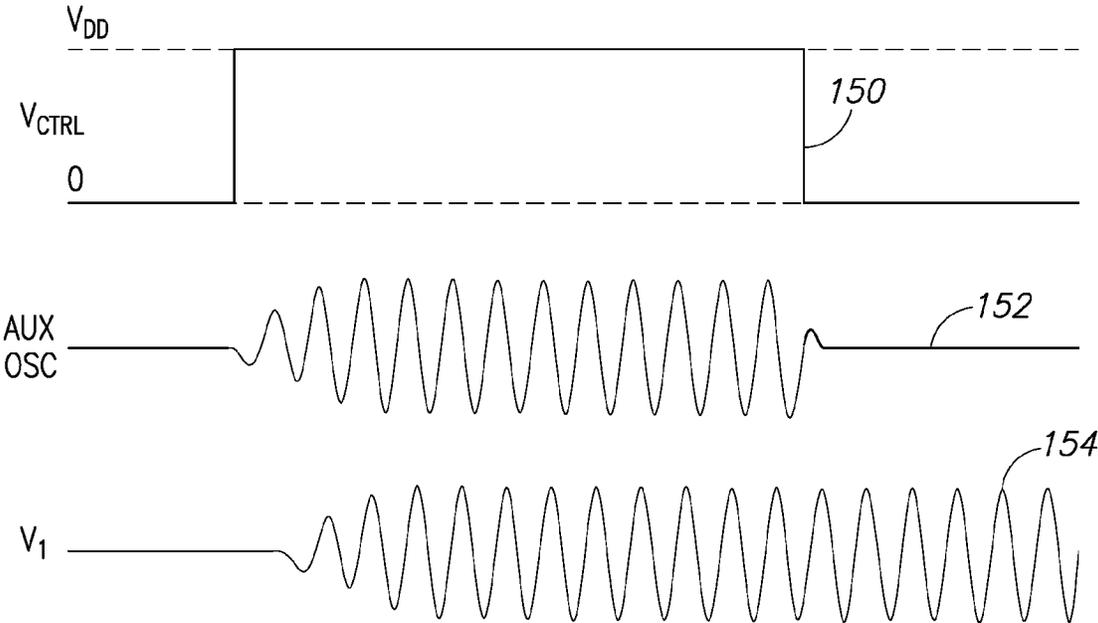
FIG.9B

FIG.9C

FIG.9D

FIG.10

FIG.11

FIG.12A

FIG.12B

FIG.13

FIG.14

FIG.15

FIG.16

NODES VOLTAGES IN LOCK STAGE 1

V_{d1}	V_1	V_{d2}	V_2	V_{d3}	V_3	V_{d4}	V_4
V_{DD}	V_{DD}	GND	GND	V_{DD}	V_{DD}	GND	GND

FIG.17A

FIG.17B

250

V_{DD} V_{DD} V_{DD} V_{DD}

M_{1p} M_{2p} M_{3p} M_{4p}

V_{d1} L_1 V_1 V_{d2} L_2 V_2 V_{d3} L_3 V_3 V_{d4} L_4 V_4

M_{1n} C_1 M_{2n} C_2 M_{3n} C_3 M_{4n} C_4

256   258   252

V_{CTRL}

260

T-GATE

254

262

AUXILIARY OSCILLATOR

FIG.18A

V_{DD}

V_{CTRL}

0

264

266

AUX
OSC

268

V_1
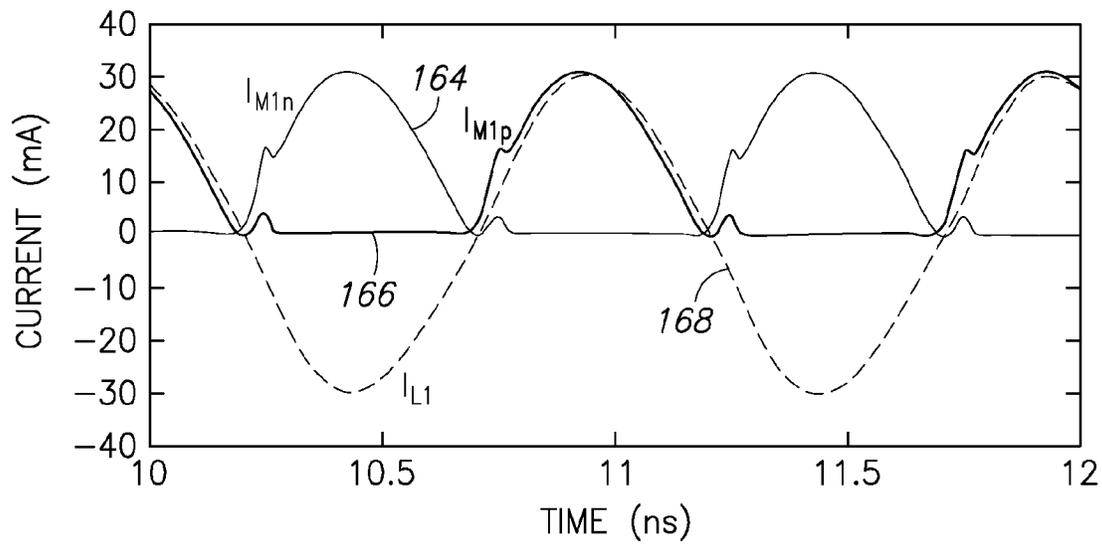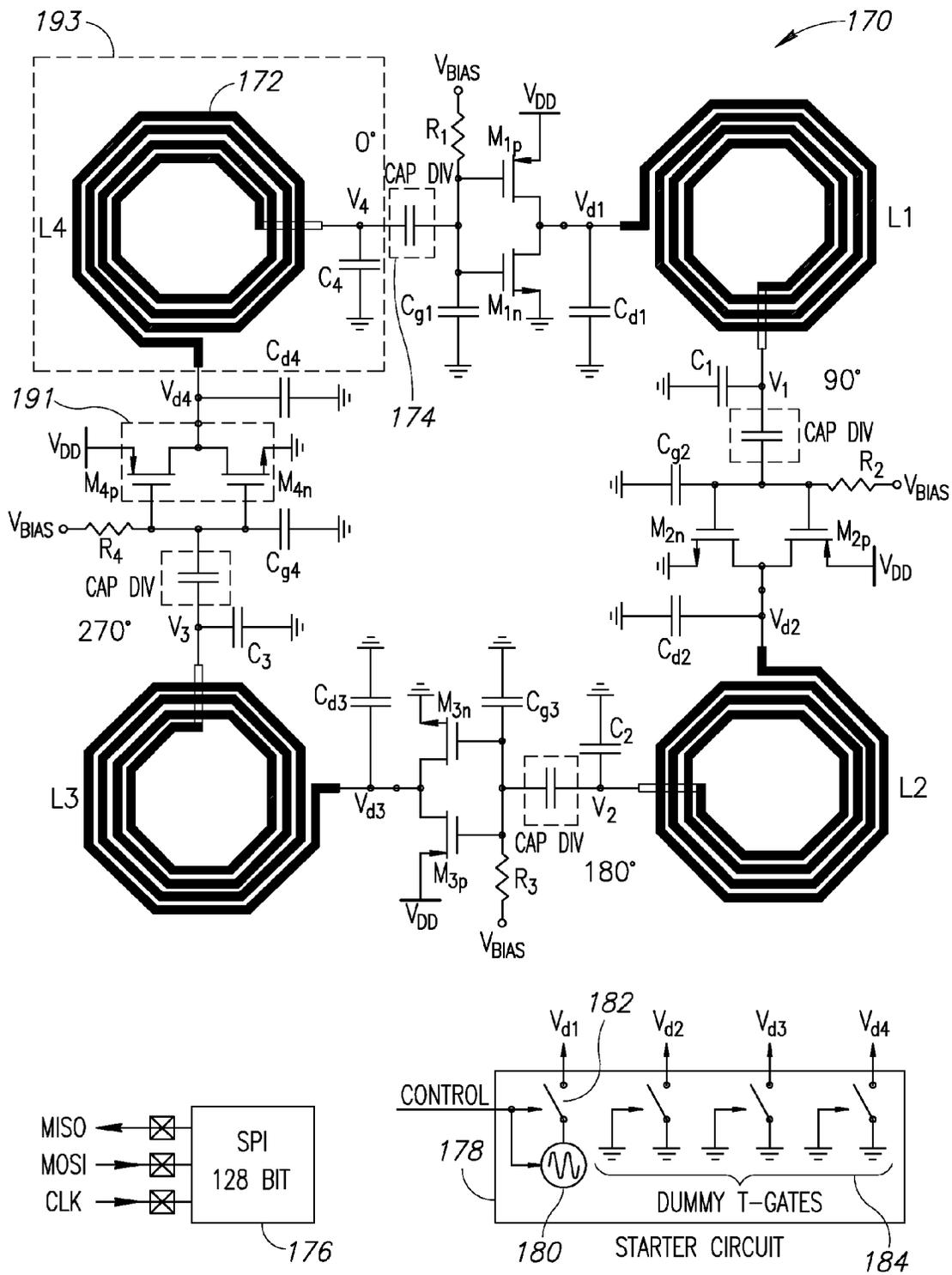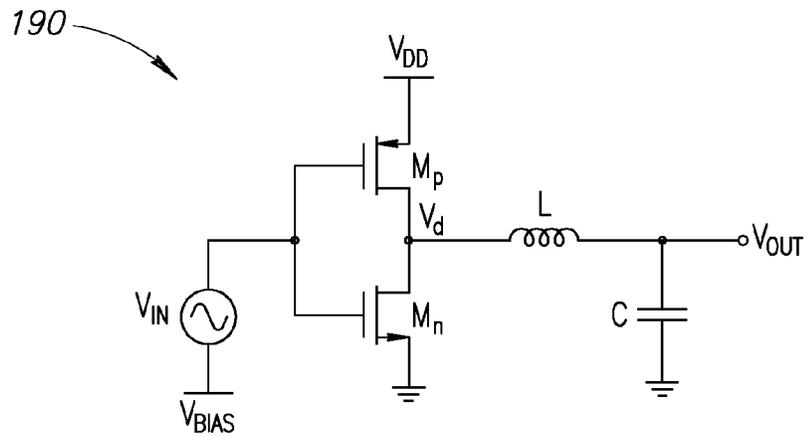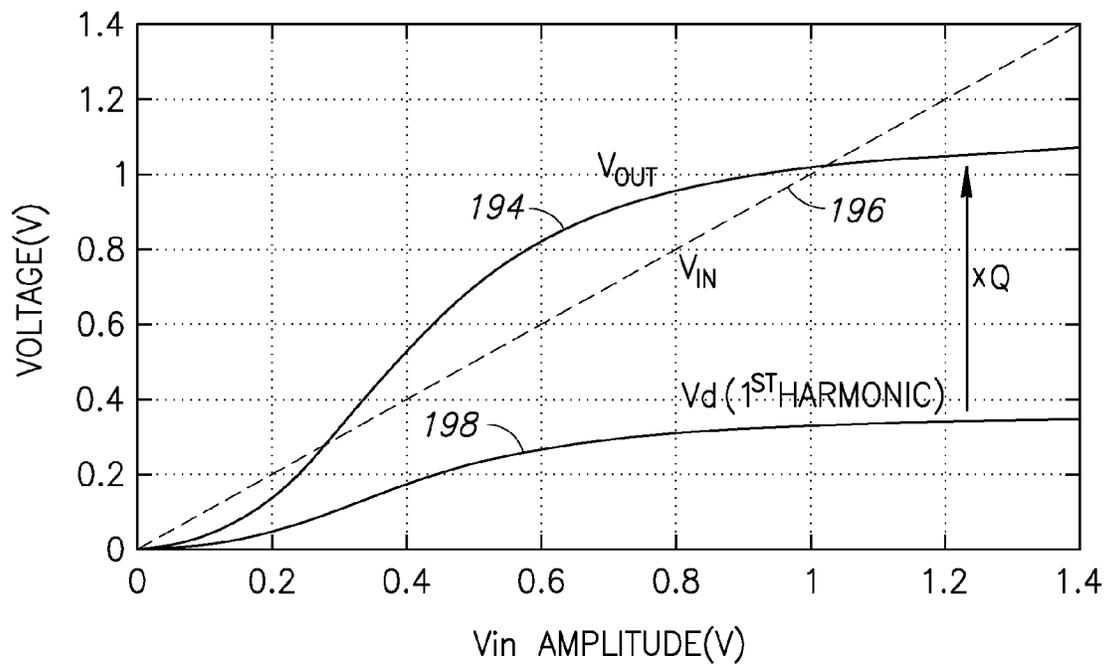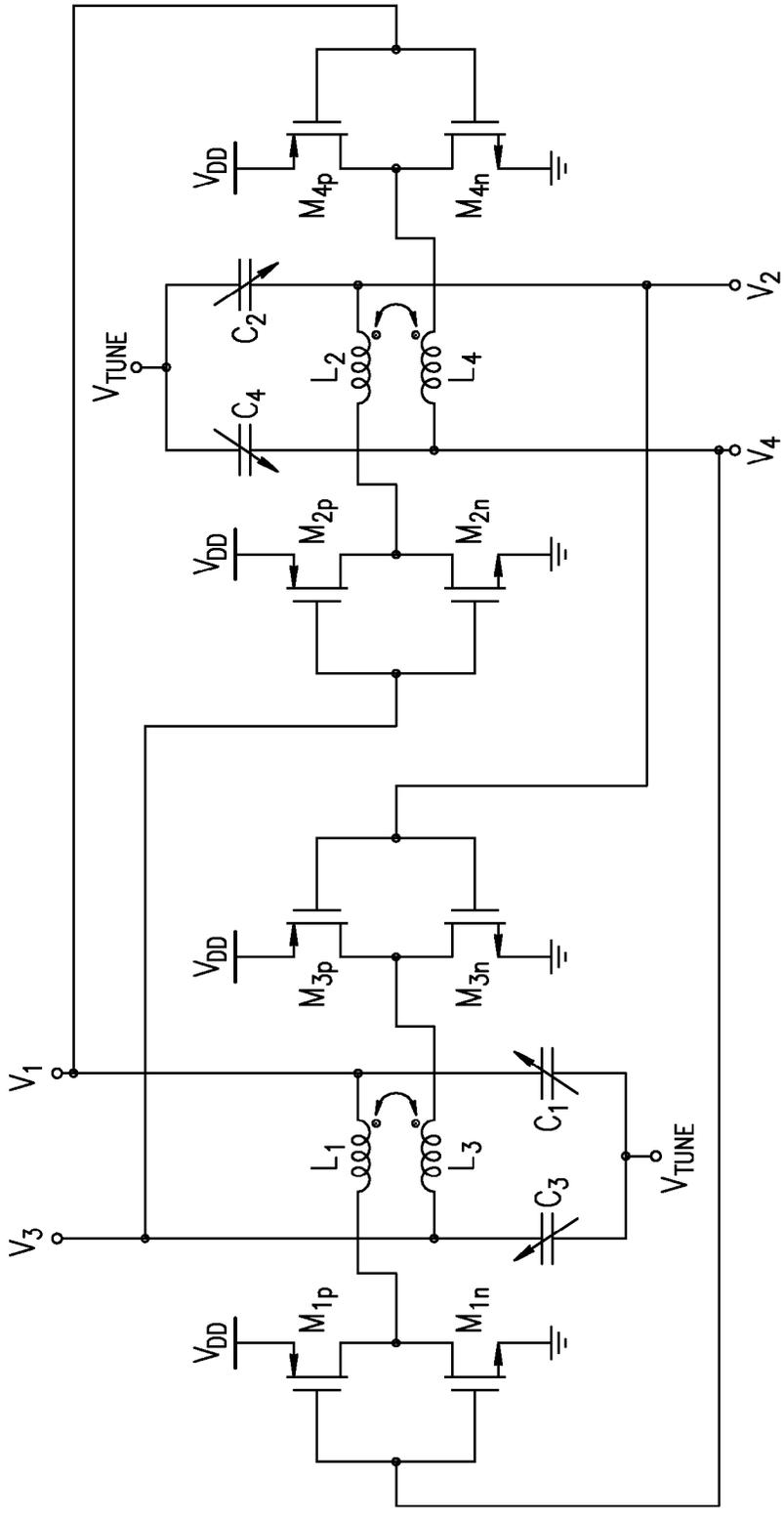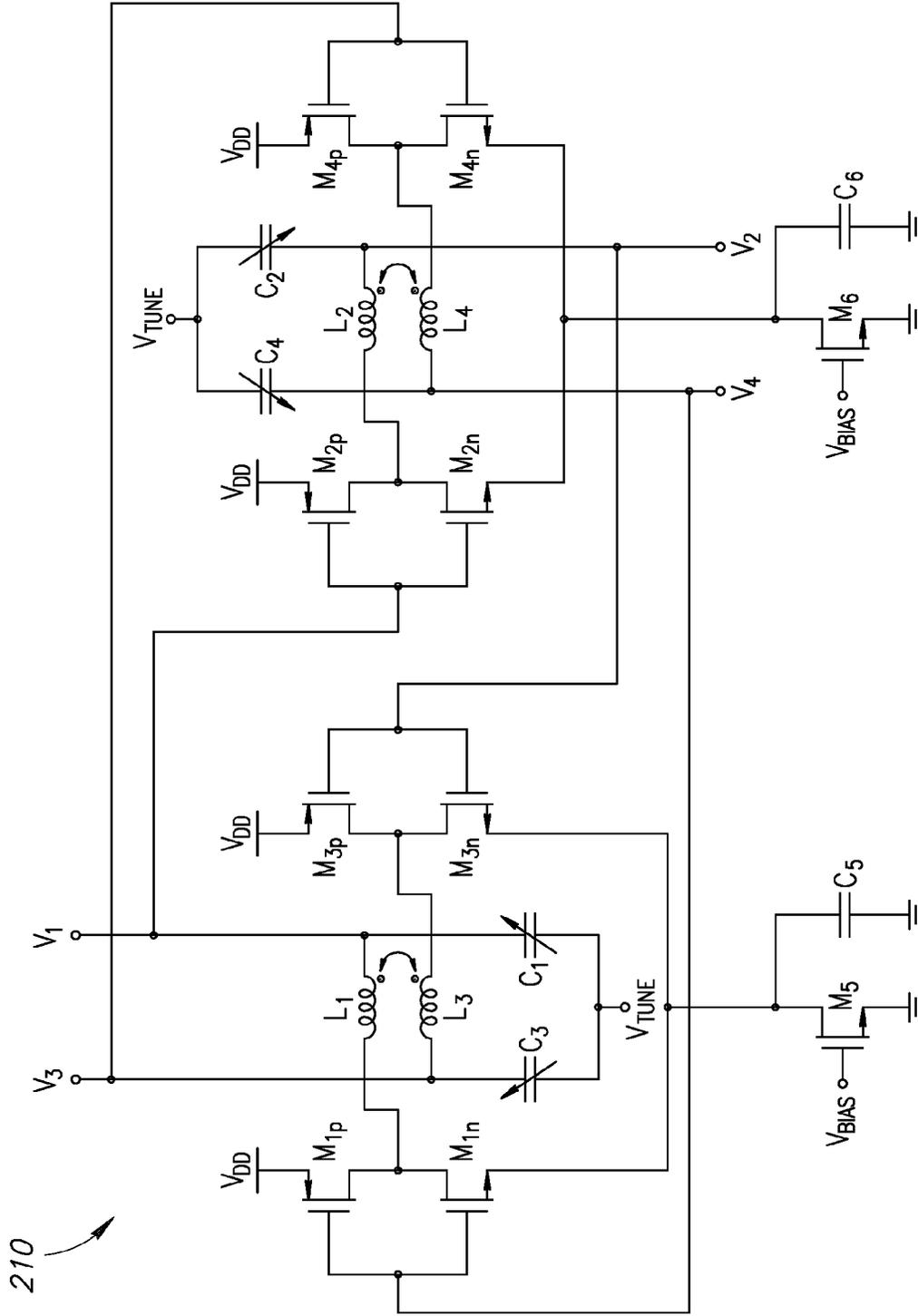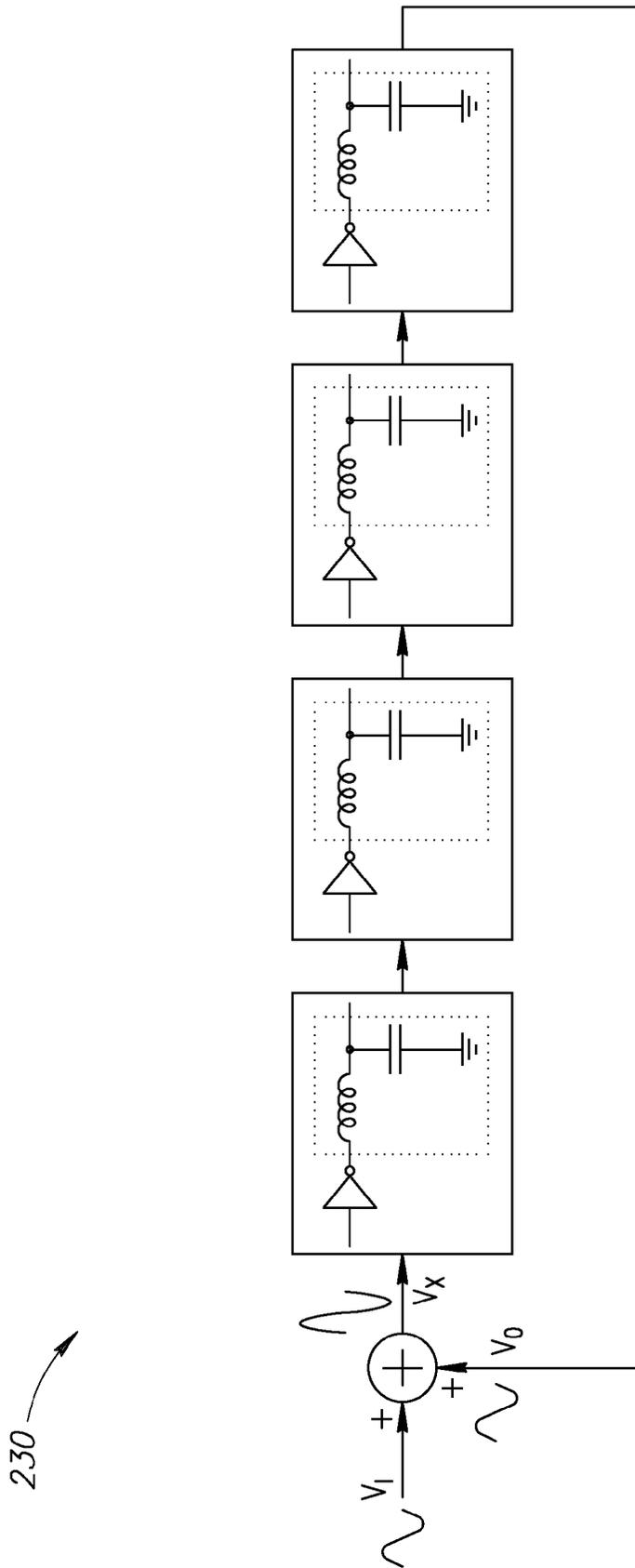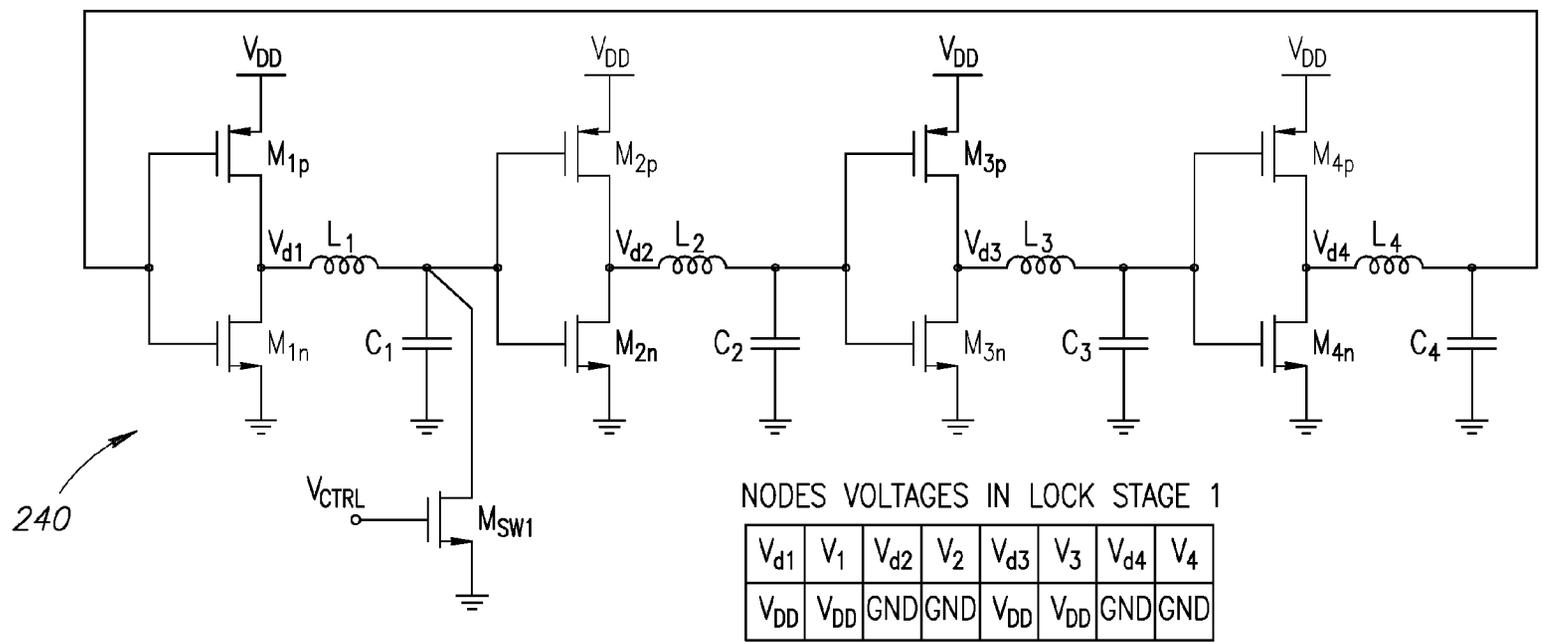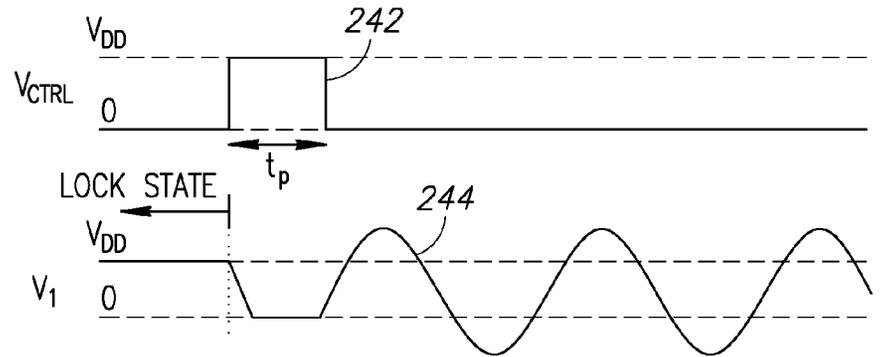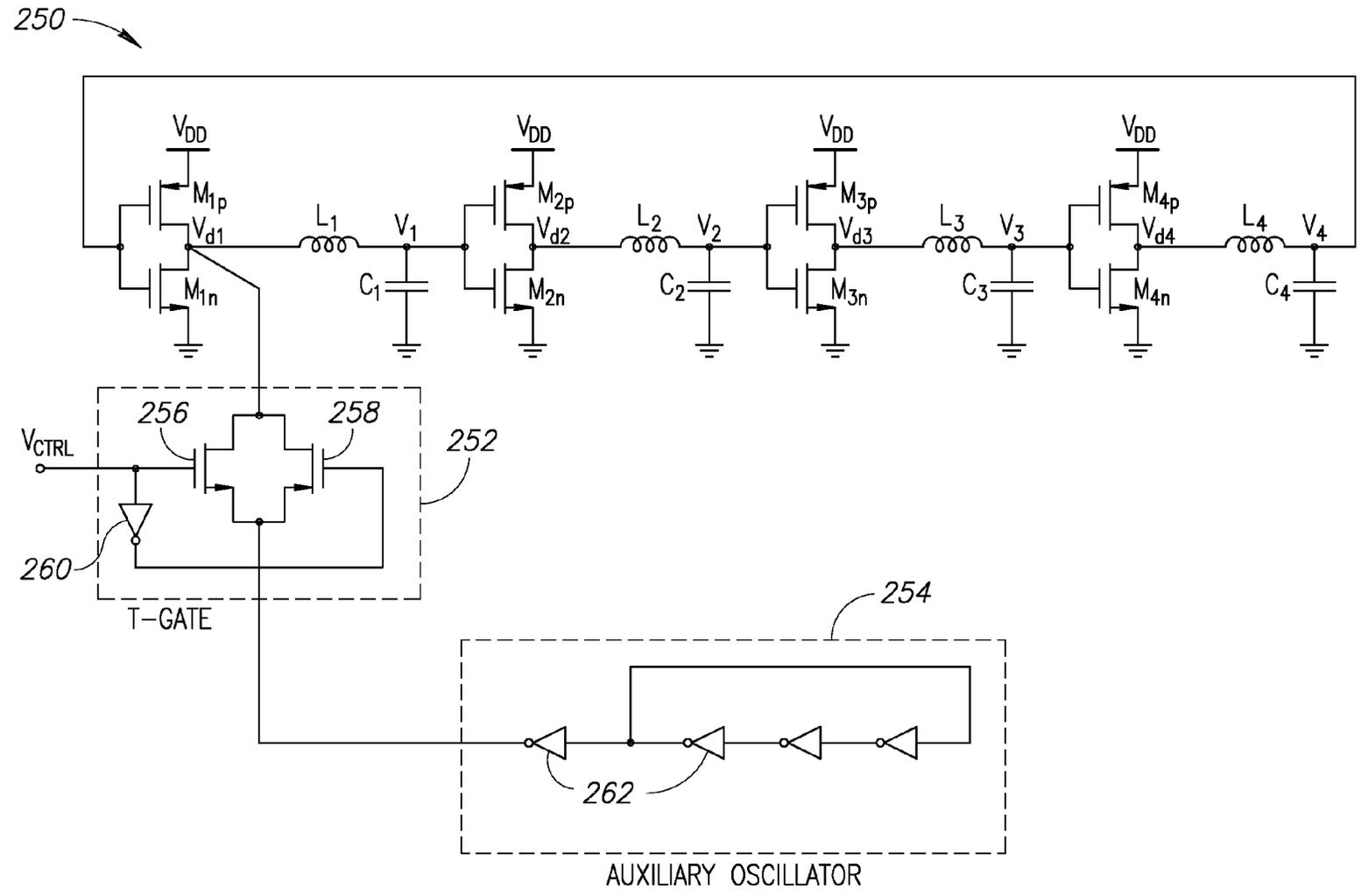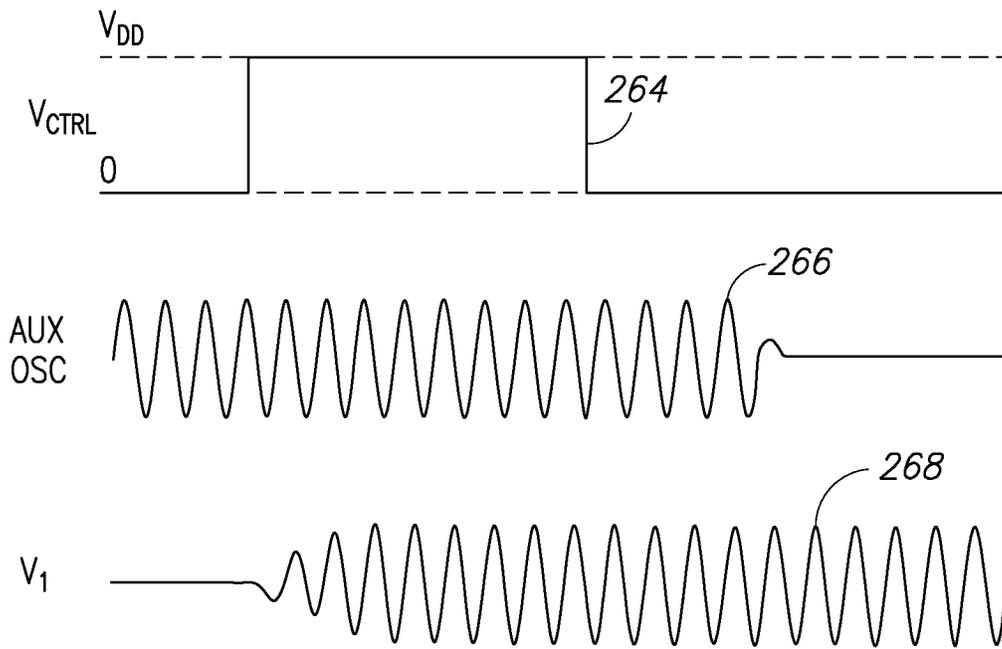
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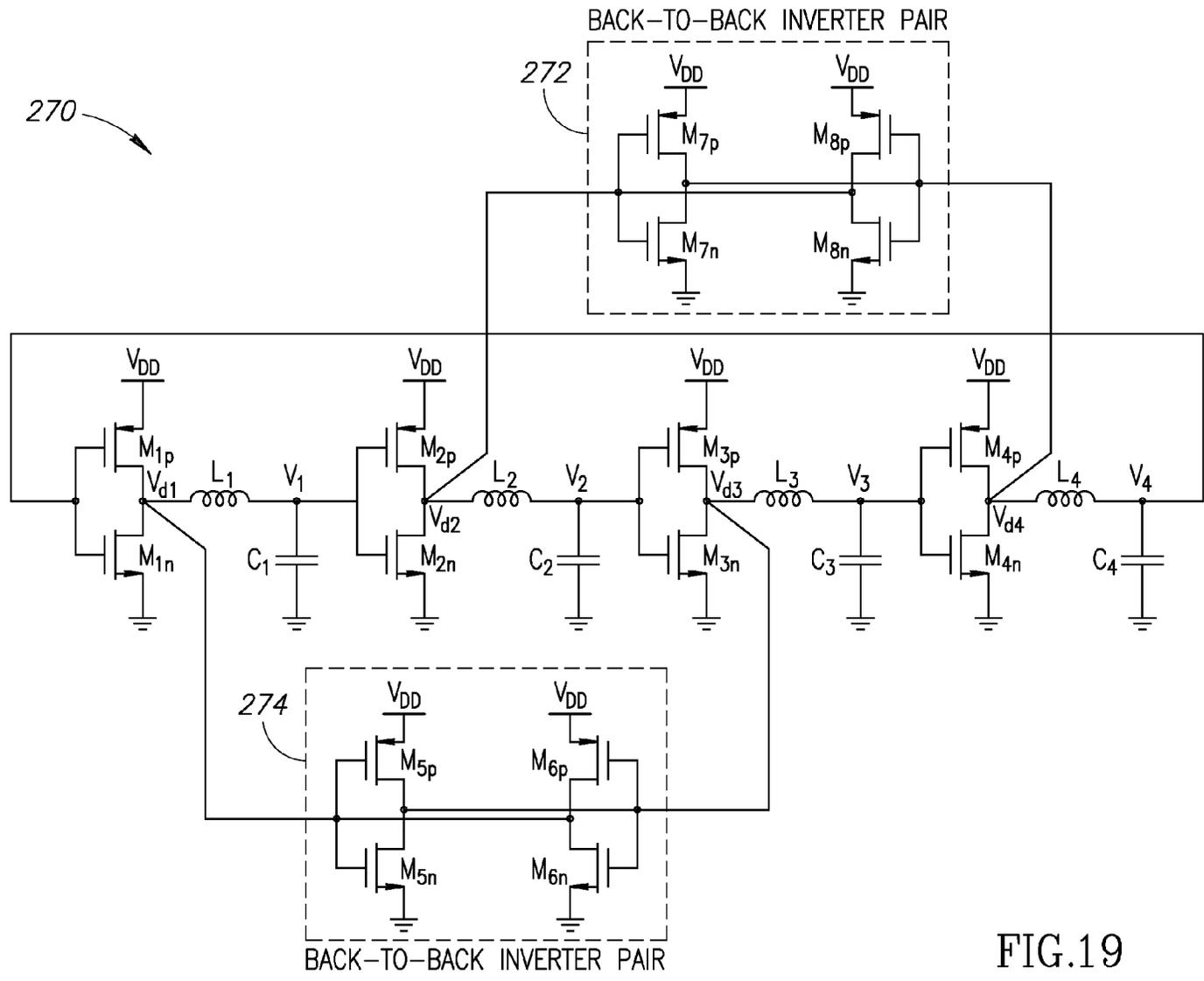
FIG.19

QUADRATURE LC TANK DIGITALLY CONTROLLED RING OSCILLATOR

REFERENCE TO PRIORITY APPLICATION

This application claims priority to U.S. Provisional Application Ser. No. 62/016,399, filed Jun. 24, 2014, entitled "Series LC Ring Oscillator," incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

The present invention relates generally to digitally controlled oscillators (DCO) and in particular to a quadrature LC tank based digitally controlled ring oscillator.

BACKGROUND OF THE INVENTION

Clock generator circuits are well known circuits that are used in a myriad of applications. In modern integrated wireless/wireline receivers, transmitters and transceivers, as well as digital processors and system-on-chip (SoC) circuits, clock generator circuits are an essential block. In particular, quadrature clock generator circuits are often used to generate multiple clock signals 90 degrees apart from each other. To reach a very high data rate in clock and data recovery integrated circuits, a multiphase oscillator is typically used. A common way to generate quadrature clock signals, is to use a conventional ring oscillator. In ring oscillators, oscillation is made based on inverter delay with capacitive and/or resistive load. A drawback with these types of oscillators though is that the phase noise is relatively high compared to LC type of oscillators.

A circuit diagram illustrating an example prior art LC type oscillator with quadrature outputs is shown in FIG. 1. The oscillator, generally referenced 10, comprises two cross coupled LC oscillators, namely oscillator A and oscillator B. The first oscillator is coupled in-phase to the second, but the second one is coupled anti-phase to the first. MOS transistors are used as the coupling devices. This idea can be extended by coupling a higher number of oscillators as shown in FIG. 2. A circuit diagram illustrating an example prior art LC type oscillator with an additional number of oscillators is shown in FIG. 2. The structure, generally referenced 20, allows an additional number of different phases to be generated.

In the oscillators of FIGS. 1 and 2, coupling the oscillators forces the oscillation frequency to be shifted away from the resonant frequency of each LC tank. Therefore, each tank shows a lower quality factor Q. In this way, quadrature accuracy can be traded-off with phase noise. The higher the coupling strength the better the in-phase/quadrature (IQ) phase accuracy, but the worse the oscillation phase noise.

A circuit diagram illustrating an example prior art multiphase LC type ring oscillator is shown in FIG. 3A. A circuit diagram illustrating an example implementation of each stage of the oscillator of FIG. 3A in more detail is shown in FIG. 3B. FIG. 3A shows a multiphase LC ring oscillator, generally referenced 30, that utilizes a parallel LC tank instead of a resistive/capacitive load as used in prior art conventional ring oscillators. The circuit, generally referenced 40, for each stage of oscillator 30 is shown in FIG. 3B.

Since it has a much higher open loop Q than the conventional ring oscillator, it has substantially better phase noise performance for the same current consumption. Compared to the oscillator of FIG. 1, cross-coupled pairs are eliminated in the structure of FIG. 3A to avoid potential parasitic

oscillation modes. In this oscillator structure, oscillation frequency is still different than the resonant frequency of each LC tank. Therefore, each LC tank shows a lower quality factor resulting in a worse phase noise. In the above three types of prior art oscillators (i.e. FIGS. 1, 2, and 3A), active coupling devices inject a current into an LC tank that is not in-phase with the voltage of the tank. Consequently, noise from the coupling device is converted to phase noise with a higher gain, compared to the case where injected current is in-phase with the voltage of the tank.

A circuit diagram illustrating an example prior art rotary traveling-wave oscillator (RTWO) is shown in FIG. 4. The structure of the RTWO, generally referenced 50, is the rotary ring composed of a differential transmission line and several active devices to compensate losses. As a wave starts to propagate around the loop, it travels 360 degrees in each rotation cycle. The use of high quality passive resonators (especially the inductors and transmission lines) results in better phase noise performance compared to a conventional ring oscillator. As transistors of the inverters enter the triode region, however, the total quality factor Q of the resonator decreases and consequently degrades phase noise performance. Note that an alternative version of the RTWO can be implemented using lumped components.

A circuit diagram illustrating an example prior art multiphase LC type ring oscillator is shown in FIG. 5A. A circuit diagram illustrating an example implementation of a negative G_m cell stage of the oscillator of FIG. 5A in more detail is shown in FIG. 5B.

In this implementation, the oscillator, generally referenced 60, comprises negative G_m elements that are each implemented by a pair of current biased inverters shown in circuit 70 in FIG. 5B. In this manner, the inverters do not load the quality factor Q of the tank. The resonant frequency of the oscillator of FIG. 5A is less than the resonant frequency of a single LC tank, making it less attractive for high frequency applications.

A circuit diagram illustrating an example prior art multiphase ring oscillator using a CL ladder configuration is shown in FIG. 6. The oscillator, generally referenced 80, is constructed as a multiphase oscillator. This oscillator uses a CL ladder rather than an LC ladder by swapping the positions of L and C. It can be shown that in an eight phase oscillator, the CL ladder configuration provides a higher resonant frequency than a LC ladder. In addition, the oscillation frequency of this oscillator is higher than the resonant frequency of a single CL tank. The oscillation frequency, however, cannot go above the resonant frequency of the inductor and parasitic parallel capacitance of the active devices.

A circuit diagram illustrating an example prior art LC delay line oscillator is shown in FIG. 7A. A circuit diagram illustrating an example implementation of a gain stage of the oscillator of FIG. 7A in more detail is shown in FIG. 7B. The oscillator structure, generally referenced 90, comprises an LC delay line oscillator configuration. In this structure, four LC delay lines are used in a loop, with each delay line driven by a gain stage 100 shown in FIG. 7B.

In this circuit, the output load resistance of the gain stage matches the characteristic impedance of the delay line. In this oscillator, most of delay around the oscillator loop is provided by the delay line, making the VCO resistant to variations in power supply, temperature and process. The oscillator frequency is the same as the resonant frequency of the LC delay line. The use of an LC tank improves the phase noise of this structure compared to conventional ring oscil-

lators. The use of resistively loaded gain stages, however, introduces extra loss in the oscillator, making it less power and phase noise efficient.

There is thus a need for an oscillator that overcomes the disadvantages of the prior art oscillator circuits. Preferably, the oscillator is able to generate quadrature phase output signals, is simple and accurate, exhibits low phase noise, has a low cost of manufacturing, is power efficient and consumes relatively little semiconductor real estate.

SUMMARY OF THE INVENTION

The present invention is a quadrature LC tank based digitally controlled ring oscillator (DCO). The oscillator structure incorporates a plurality of stages, each stage including an inverter and a series LC tank. Four stages are coupled together to create a 360 degree phase shift around a loop. The oscillation frequency of the oscillator is the same as the resonant frequency of each LC tank, therefore it avoids quality factor degradation of LC tanks found in the prior art. In one example embodiment, class-D amplifiers are used to drive each of the LC tanks. Capacitor banks at the input and output of the buffers provide coarse and fine tuning of the frequency of oscillation. The high efficiency exhibited by these amplifiers results in very good phase noise performance of this oscillator. The oscillator utilizes a startup circuit to launch oscillation upon power on.

There is thus provided in accordance with the invention, a ring oscillator comprising a plurality of phase shifters configured in a loop, a plurality of active circuits, each active circuit coupled to and associated with one of the phase shifters and wherein a gain of the plurality of active circuits combined with voltage amplification of the phase shifters causes the loop to oscillate.

There is also provided in accordance with the invention, a ring oscillator comprising a plurality of LC-tank based phase shifters configured in a loop, a plurality of amplifiers, each amplifier coupled to and associated with one of the phase shifters, wherein the gain of the plurality of amplifiers combined with voltage amplification of the phase shifters is sufficient to maintain oscillation in the loop and a startup circuit operative to inject one or more pulses into the loop to launch the oscillation.

There is further provided in accordance with the invention, a quadrature ring oscillator comprising a plurality of four 90 degree phase shifters configured in a loop, a plurality of four active circuits, each active circuit coupled in series with one of the phase shifters, a plurality of tuning capacitors, each tuning capacitor coupled to and associated with one of the active circuits, wherein a gain of the plurality of active circuits combined with voltage amplification of the phase shifters is sufficient to maintain oscillation in the loop and a startup circuit operative to inject one or more pulses into the loop to launch the oscillation.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is herein described, by way of example only, with reference to the accompanying drawings, wherein:

FIG. 1 is a circuit diagram illustrating an example prior art LC type oscillator with quadrature outputs;

FIG. 2 is a circuit diagram illustrating an example prior art LC type oscillator with an additional number of oscillators;

FIG. 3A is a circuit diagram illustrating an example prior art multiphase LC type ring oscillator;

FIG. 3B is a circuit diagram illustrating an example implementation of each stage of the oscillator of FIG. 3A in more detail;

FIG. 4 is a circuit diagram illustrating an example prior art rotary traveling-wave oscillator;

FIG. 5A is a circuit diagram illustrating an example prior art multiphase LC type ring oscillator;

FIG. 5B is a circuit diagram illustrating an example implementation of a negative G_m cell stage of the oscillator of FIG. 5A in more detail;

FIG. 6 is a circuit diagram illustrating an example prior art multiphase ring oscillator using a CL ladder configuration;

FIG. 7A is a circuit diagram illustrating an example prior art LC delay line oscillator;

FIG. 7B is a circuit diagram illustrating an example implementation of a gain stage of the oscillator of FIG. 7A in more detail;

FIG. 8A is a circuit diagram illustrating an example series LC tank used as 90 degree phase shifter;

FIG. 8B is a circuit diagram illustrating an example implementation of the driving buffer in the circuit of FIG. 8A in more detail;

FIG. 8C is a graph illustrating magnitude response versus frequency for the circuit of FIG. 8A;

FIG. 8D is a graph illustrating phase response versus frequency for the circuit of FIG. 8A;

FIG. 9A is a circuit diagram illustrating an example embodiment of the class-D series LC tank ring oscillator with a starting circuit constructed in accordance with the present invention;

FIG. 9B is a diagram illustrating example waveforms of the circuit of FIG. 9A;

FIG. 9C is a graph illustrating voltage versus time for the circuit of FIG. 9A;

FIG. 9D is a graph illustrating current versus time for the circuit of FIG. 9A;

FIG. 10 is a circuit diagram illustrating a second embodiment of the ring oscillator of the present invention;

FIG. 11 is a circuit diagram illustrating a third embodiment of the ring oscillator of the present invention;

FIG. 12A is a circuit diagram illustrating one of the stages of the ring oscillator in more detail;

FIG. 12B is a graph illustrating output versus input amplitude of one of the stages of the ring oscillator;

FIG. 13 is a circuit diagram illustrating a fourth embodiment of the ring oscillator of the present invention having mutual coupling between inductors;

FIG. 14 is a circuit diagram illustrating a fifth embodiment of the ring oscillator of the present invention having a differential configuration with tail current sources;

FIG. 15 is a circuit diagram illustrating a sixth embodiment of the ring oscillator of the present invention incorporating capacitive voltage dividers;

FIG. 16 is a circuit diagram illustrating an example feedback system of the ring oscillator of the present invention;

FIG. 17A is a circuit diagram illustrating a seventh embodiment of the ring oscillator of the present invention incorporating a startup circuit that injects a short pulse to the oscillator loop;

FIG. 17B is a diagram illustrating example waveforms of the circuit of FIG. 17A;

FIG. 18A is a circuit diagram illustrating an eighth embodiment of the ring oscillator of the present invention incorporating a startup circuit that includes an auxiliary oscillator;

FIG. **18**B is a diagram illustrating example waveforms of the circuit of FIG. **18**A; and

FIG. **19** is a circuit diagram illustrating a ninth embodiment of the ring oscillator of the present invention incorporating a startup circuit that includes back to back inverter pairs.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is a quadrature LC tank based digitally controlled ring oscillator. Note that, alternatively, one skilled in the art can implement analog tuning for use in analog PLLs. The oscillator structure incorporates a plurality of LC tanks, such as four, to create a 360 degree phase shift around a loop. The oscillation frequency of the oscillator is the same as the resonant frequency of each LC tank, therefore it avoids quality factor degradation of LC tanks found in the prior art. In one example embodiment, class-D amplifiers are used to drive each of the LC tanks. The high efficiency exhibited by these amplifiers results in very good phase noise performance of this oscillator. The oscillator utilizes a startup circuit to launch oscillation upon power on.

The phase noise exhibited by an oscillator is among the most important criterion of an oscillator. In addition to phase noise (PN), important performance criteria include the active area, fine tuning steps and high phase accuracy which are also critical in many applications. While minimizing PN, the focus is also typically on cost and area. Most communication systems require high accuracy quadrature clocks. Ultrafine tuning steps are also required to reach a high modulation accuracy and low quantization noise in a digitally controlled oscillator that is part of a digital PLL.

In one embodiment, the present invention is a quadrature series LC tank ring oscillator (RO) that uses high-efficiency class-D amplifiers. A first DCO constructed in accordance with the present invention uses ultra-small low-Q inductors to achieve a very low semiconductor area while maintaining high purity referred to as the "LA" version. A second DCO constructed in accordance with the present invention uses larger inductors to achieve very low phase noise while featuring very high I/Q accuracy and ultra-fine tuning steps referred to as a high-performance or "HP" version.

A circuit diagram illustrating an example series LC tank used as 90 degree phase shifter is shown in FIG. **8**A. A circuit diagram illustrating an example implementation, generally referenced **116**, of the driving inverter on the circuit of FIG. **8**A in more detail is shown in FIG. **8**B. A graph illustrating magnitude response versus frequency for the circuit of FIG. **8**A is shown in FIG. **8**C. A graph illustrating phase response versus frequency for the circuit of FIG. **8**A is shown in FIG. **8**D.

With reference to FIG. **8**A, a series LC tank, generally referenced **110**, is driven by a low impedance source. A Bode plot **112** in FIGS. **8**C and **8**D shows the output voltage of this LC tank circuit amplified Q times and phase shifted by −90 degrees (see plot **114**) at the resonant frequency of the LC tank. To work properly, the tank is preferably driven with a low impedance source. A simple CMOS inverter **118** as a class-D amplifier provides such a low impedance as long as a sufficiently large enough input signal is provided as shown in FIG. **8**B. While the input of the inverter is a sinusoidal signal, its output jumps rapidly between 0V and V_{DD} yielding a square wave. The LC tank filters higher harmonics and generates a sinusoidal with total phase shift of +90 degrees with respect to the inverter's input. Putting a plurality of these stages in a loop, e.g., four, a 360 degree phase

shift is generated with sufficient gain to satisfy the Barkhausen criterion of oscillation.

In one embodiment, the architecture of the oscillator is based on a 90 degree phase shifter. Using a multiple, e.g., four, of these phase shifters in a loop with the required amplification gain, Barkhausen phase and gain criteria can be satisfied and a quadrature oscillator is formed. The simplest 90 degree phase shifter is a series LC tank. Plots **112** and **114** of FIGS. **8**C and **8**D, respectively, show the frequency response of this network.

This second-order low-pass filter produces an exact 90 degree phase shift at resonance frequency. Moreover, it has a voltage gain equal to the quality factor (Q) of the tank. To maintain the quality factor of the tank, it is preferably driven with a low impedance voltage source. Also, its output load is preferably a high impedance or capacitive load to be absorbed as part of the tank capacitance.

A circuit diagram illustrating an example embodiment of the class-D series LC tank ring oscillator with a starting circuit constructed in accordance with the present invention is shown in FIG. **9**A. A diagram illustrating example waveforms of the circuit of FIG. **9**A is shown in FIG. **9**B. A graph illustrating voltage versus time for the circuit of FIG. **9**A is shown in FIG. **9**C. A graph illustrating current versus time for the circuit of FIG. **9**A is shown in FIG. **9**D.

The core of the oscillator, generally referenced **120**, is shown in FIG. **9**A. If there is an oscillation in the loop, the core maintains it and creates 0, 90, 180, and 270 degree phases. If the oscillator starts from zero, however, positive DC gain around the loop forces the outputs of the inverters to 0 and V_{DD} (e.g., $V_{d1}=V_{d3}=0$ and $V_{d2}=V_{d4}=V_{DD}$). In this state, the oscillator is locked and the gain of the inverters is around zero. Therefore, unlike in conventional oscillators, noise does not initiate the oscillation build-up. The present invention incorporates a starter circuit operative to generate the initial oscillation in the core. In one embodiment, the starter circuit includes an auxiliary oscillator **124** at a frequency roughly near resonant frequency of the core as well as a T-gate circuit **122** that connects it to the core. At first, the auxiliary oscillator **124** is turned on and connected to the core. After few nanoseconds when oscillation is established in the main core, the auxiliary oscillator is turned off and disconnected. Adding back-to-back inverters **126** between the differential outputs (i.e. $V_{d1,3}/V_{d2,4}$) assists easier startup of the core.

FIG. **9**B shows transient waveforms of the oscillator including V_{ctrl} **150**, Aux Osc **152** and V_1 **154**. If the inverters **121** are sized properly, the voltage waveform of their outputs comprises a square wave. Then, each of the transistors conducts when only its drain-source voltage is about zero. In this way the inverters are operated as high-efficiency class-D amplifiers without noticeable degradation of the tank Q-factor.

In one embodiment, the oscillator **120** comprises four series LC tanks **123** and four inverters **121** in a loop. The four LC tanks provide approximately 360 degree phase shift around the loop, with 90 degrees generated by each tank. The required loop gain for oscillation is provided by voltage amplification of the series LC tank in combination with gain of the inverters. The four inverters ensure proper driving of the LC tanks with a low impedance as well as isolating them. In general, active circuits or buffers are used in place of inverters. Furthermore, the capacitive input impedance of the inverter is absorbed by the capacitor of the LC tank. One skilled in the art, however, can implement the buffers in other ways besides inverters to achieve the oscillator of the present invention.

FIGS. **9C** and **9D** show simulated voltage and current waveforms of the oscillator with V_{DD}=0.6V and Q=3, at 1 GHz. Note that it is assumed that the oscillator **120** has proper initial conditions and a stable oscillation. In this state, the inverters have a full swing square wave output (V_{d1}-V_{d4}) between 0 and V_{DD}. The first LC tank filters higher harmonics of its square wave input (V_{d1}) **162** resulting in a sine wave output on V_1 **158**. Since the circuit oscillates at resonance frequency of the tanks, V_1 has a –90° phase shift relative to V_{d1}. Furthermore, the amplitude of V_1 is Q times larger than the first harmonic of V_{d1}. Next, V_1 drives the subsequent buffer in the chain which converts its sine wave input into an inverted square wave (V_{d2}) **160** which results in a sine wave output on V_2 **156**. This sequence continues in the loop for the subsequent stages.

By having a large enough voltage swing at the input of each inverter and appropriate transistors sizes, the outputs of the inverters are square waves switching rapidly between 0 and V_{DD}. In this manner, while each of the NMOS or PMOS transistor is on, its drain to source voltage drop is nearly zero. Therefore, the inverters are operating as very high efficiency class-D amplifiers with very low power loss. Consequently, most of oscillator input power is injected into the LC tanks yielding large oscillation amplitude and low phase noise.

Considering (expediently) buffers as ideal amplifiers with a small-signal negative gain A, the transfer function of the open loop can be written as follows:

$$H(j\omega) = \left(\frac{-A}{1 + jRC\omega - LC\omega^2} \right)^4 \qquad (1)$$

in which R, L and C are series loss resistance, inductance and capacitance of the tank, respectively. Consequently, the oscillation frequency can be calculated as:

$$\omega_{OSC} = \frac{1}{\sqrt{LC}} \qquad (2)$$

which is the same resonance frequency of each individual tank.

A circuit diagram illustrating a second embodiment of the ring oscillator of the present invention is shown in FIG. **10**. The oscillator, generally referenced **170**, comprises a plurality of stages, e.g., four, with each stage comprising a buffer **191** coupled to an LC tank **193**. In this example, the buffer comprises an inverter and the LC tank comprises L_{1-4} **172** and C_{1-4}. Note that capacitors C_{g1-4} and the parasitics of subsequent inverters can be also considered as part of C_{1-4}. The oscillator also comprises starter circuitry **178** and an I/O interface **176** for configuring the capacitor selection which controls the coarse and fine tuning of the frequency of oscillation. The startup circuitry comprises an auxiliary oscillator **180**, T-gate **182** and dummy T-gates **184**.

In one embodiment, the oscillator **170** utilizes four relatively small inductors to save area. Consequently, the inductors have a very low quality factor of about 1.5 to 2. In another embodiment, the oscillator uses four regular size inductors with Q≈8. Since the series LC tank at resonance has a voltage amplification gain of Q for the first harmonic, its voltage swing can break down the gate oxide of inverters. Therefore, capacitor **174** is placed before each inverter to make a capacitive voltage divider in combination with

parasitic capacitance of the inverter. Then, by choosing an appropriate capacitor value, the voltage swing at the input of the inverter is reduced to a value ensuring reliability of the transistors. In this embodiment, the gate of the transistors is biased through R_{1-4} to V_{bias} which comes from a dummy self-biased inverter. In addition to the starter circuit, three dummy switches are placed at the output of the other inverters to keep the four phases balanced.

It is noted that the quadrature oscillator structure can reach a relatively high I/Q accuracy, as the 90 degree phase shifts are inherently generated around the loop. In contrast, prior art QVCOs made by cross coupling two oscillator cores trades off quadrature accuracy with PN. Due to the single ended implementation of the oscillator of the present invention, no layout asymmetry is created that would otherwise degrade I/Q accuracy. To measure the oscillator quadrature accuracy, four quadrature baseband signals are upconverted by the oscillator quadrature signals around the carrier. Image rejection ratio (IMRR) of the upconverted signal reflects the quadrature accuracy of the oscillator. The image rejection ratio (IMRR) is measured for the high-performance (HP) version of the oscillator across the tuning range. In one example, IMRR ranges from 45 to 60 dB for the HP version and from 35 to 47 dB for the LA version, considering worst case out of 5 IC samples each.

Note that the preferred way to tune the frequency of oscillation is by changing the capacitances in series with the inductors. In the LA version, C_{1-4} (FIG. **11**) is tunable by 5 bits of 12 fF steps, covering an octave (66%) tuning range from 2.82 to 5.61 GHz. In the HP version, coarse tuning banks C_{1-4} (FIG. **10**) are tunable by 4 bits of 20 fF steps. This covers a tuning of 26% from 1.85 to 2.4 GHz. In addition to these banks, four fine tuning banks are added (C_{g1-g4} in FIG. **10**). Each of these capacitor banks are 7 bits with an ultralow step size of 100 aF. This gives a frequency resolution of 20 kHz in 500 steps ($\approx 4 \times 2^7$ levels), when fine tuning banks are controlled separately.

To achieve further ultrafine tuning steps, capacitor banks C_{d1-d4} (FIG. **10**) can be placed at the inverter outputs. Any capacitance at the output of each inverter introduces a small delay inversely proportional to the large-signal G_m of the inverter. As the inverters are very strong to be able to drive the LC tanks, the capacitance effect at the output of inverters in much smaller than its effect when it is paralleled with C_{1-4}. Placing the same fine tuning banks at the output of inverters (C_{d1-d4} in FIG. **10**) improves the frequency resolution down to 1.27 kHz, i.e. a 16× reduction in this example implementation.

Thus, the tank capacitor bank C_{1-4} provides relatively coarse frequency tuning of the oscillator. Capacitor bank C_{g1-4} connected to the input of the buffers provides somewhat finer tuning resolution. Capacitors C_{d1-4} connected to the output of the buffers, however, provide extremely fine tuning, e.g., 1.27 kHz. This capacitor bank at the drains of the buffers, however, has much less effect than the capacitor bank connected to the gate of the buffers and is able to achieve much finer resolution.

Differential nonlinearity (DNL) and integral nonlinearity (INL) of the oscillator ranges from –0.9/+0.95 and –0.86/+1 LSB, respectively. Considering the achieved DNL/INL, the frequency resolution of 1.27 kHz is extremely high. The PN and figure of merit (FoM) of the high performance oscillator versus supply voltage are also relatively good. The oscillator shows an FoM of 186.5 to 187 dB across its tuning range when V_{DD} is 0.8V. As V_{DD} goes down, voltage amplitude at the inputs of the inverters are reduced and thus output impedance of the inverters are increased. This gradually

degrades the tank quality factor and results in a lower FoM. Flicker noise of this oscillator ranges from 200 kHz to 300 kHz. The low area (LA) version oscillator, exhibits an FoM of 167.5 to 176.7 dB across its tuning range. When the oscillator is running at 5.6 GHz, the inductors have a slightly higher Q. V_{DD} is reduced from a typical 1.1V to 0.85V. Note that in both LA and HP implementations of the oscillator, the four inductors L_{1-4} are placed in a substantially symmetric manner. Since the currents of each two succeeding inductors have a 90 degree phase shift, the total magnetic field rapidly becomes zero as we move away from the oscillator core. This effect specifically reduces magnetic coupling of this structure with other blocks in the same die.

A circuit diagram illustrating a third embodiment of the ring oscillator of the present invention is shown in FIG. **11**. The oscillator, generally referenced **181**, comprises a plurality of stages, e.g., four, with each stage comprising a buffer **195** coupled to an LC tank **197**. In this example, the buffer comprises an inverter and the LC tank comprises L_{1-4} **183** and C_{1-4}. The oscillator also comprises starter circuitry **187** and an I/O interface **185** for configuring the capacitor selection which controls the coarse and fine tuning of the frequency of oscillation. The startup circuitry comprises an auxiliary oscillator **171**, T-gate **189** and dummy T-gates **173**. The oscillator also comprises back to back inverter gates **199** similar to the back to back inverters **126** of FIG. **9A**. The inverters **199** are coupled to the nodes V_{d1-d4} and are operative to assist in startup, for example in the low area (LA) version of the oscillator. The operation of the oscillator **181** is similar to that of oscillator **170** of FIG. **10** and will not be repeated here.

A circuit diagram illustrating one of the stages of the ring oscillator in more detail is shown in FIG. **12A**. A graph illustrating output versus input amplitude of one of the stages, generally referenced **190**, of the ring oscillator for V_{DD}=0.6V and Q=3, at 1 GHz is shown in FIG. **12B**. To satisfy the loop gain criteria, each of four stages preferably has a gain of 1 in the steady state. Since the quality factor of the tank is usually more than unity, the absolute large signal gain of the buffers are less than unity. In fact, they act as limiters switching between 0 and V_{DD} in steady state operation. Hence, these transistors should be large enough to switch the tanks completely.

FIG. **12B** shows the output oscillation amplitude **194** of one of the stages versus the input sine wave amplitude **196**. The input bias voltage of this stage is tuned to be the same as the output voltage. As the input amplitude increases, amplitude of V_d **198** increases as well. Since the input frequency is the same as the resonant frequency of the LC tank, V_{out} is Q times larger than the first harmonic of V_d. For large input amplitudes, V_d is saturated between 0 and V_{DD}. Therefore, the large signal gain from V_{in} to V_d is less than one. If the LC tank has a high enough quality factor, large signal gain from V_{in} to V_{out} can be higher than one. Then, the oscillator loop can have a stable oscillation. The point where the amplitude of V_{out} and the input amplitude are equal with a curve slope of less than unity is the stable output oscillation amplitude ($\approx$1.02V in this plot, see traces **194** and **196**).

A circuit diagram illustrating a fourth embodiment of the ring oscillator of the present invention having mutual coupling between inductors is shown in FIG. **13**. In this circuit, generally referenced **200**, L_1 and L_3 as well as L_2 and L_4 are magnetically coupled to act as transformers. Relatively low Q inductors are used where each coupled L is 180 degrees out of phase. Otherwise, the operation of the circuit is similar to that of the oscillator of FIGS. **10** and **11**.

A circuit diagram illustrating a fifth embodiment of the ring oscillator of the present invention having a differential configuration with tail current sources is shown in FIG. **14**. The circuit, generally referenced **210**, represents a differential embodiment with tail current sources (i.e. M_5 and M_6). To maintain class-D operation of the amplifiers, relatively large capacitors (i.e. C_5 and C_6) are connected in parallel with the current sources to make tail nodes AC ground. Using the current sources, the oscillation amplitude as well as current consumption of the oscillator can be controlled.

A circuit diagram illustrating a sixth embodiment of the ring oscillator of the present invention incorporating capacitive voltage dividers is shown in FIG. **15**. In this circuit, generally referenced **220**, capacitive voltage dividers **222** are used before each transistor stage. When a high quality factor LC tank is used, the voltage swing at the output of each LC can be several times higher than V_{DD}, damaging the transistors. Using the voltage dividers, this voltage is scaled down to an acceptable range for the transistors. The voltage dividers comprise capacitors C_{s1-4} and C_{p1-4}. Bias resistors R_1-R_4 are required to provide the DC bias voltage for the transistors. Note that the operation of this embodiment is similar to that of the oscillator **170** of FIG. **10**.

In one embodiment, the transistors of the oscillator stages are preferably sized large enough to have a small output resistance. Even though a specific amplitude can be found in which the loop has a large signal gain of more than one, this the oscillator of the present invention does not inherently tend to oscillate at startup. The reason for this is explained as follows. First consider a conventional three stage inverter based ring oscillator. In this case, the loop has a negative feedback at DC frequency. This means that all outputs remain in a metastable DC point before oscillation startup. Intrinsic noise of this three stage oscillator may find a loop gain of more than unity with zero degree phase shift at a certain frequency which causes the oscillation to build up. The noise can cause startup only in oscillators in which both amplitude and phase criteria are satisfied in small signal around the DC bias point of the circuit.

In the case of one embodiment of the oscillator of the present invention, there are four inverting stages in contrast to the previous case with three inverters. Thus, there is a positive feedback loop at DC frequency (i.e. with shorted inductors and open capacitors at this frequency) which forces the outputs of two stages to stay high and the outputs of the other two stages to stay low. Considering the example oscillator **120** of FIG. **9A**, V_{d1} and V_{d3} might remain at V_{DD} and V_{d2} and V_{d4} to ground, or vice versa. Therefore, the drain current of all the transistors will be zero disregarding leakage currents. In this lock state, although the noise may find phase shift criterion at a certain frequency, the small signal gain is quite low. Thus, the noise is not capable of gaining enough amplification to increase and make oscillation around the loop at startup. Although the lock state does not occur when the capacitor divider is present, e.g., in FIG. **10**, each stage might not have sufficient signal gain for startup. As shown in FIG. **12B**, the gain of each stage could be less than unity for small signals, while it could increase to more than unity for a large input signal (see traces **194** and **196**).

A circuit diagram illustrating an example feedback system of the ring oscillator of the present invention is shown in FIG. **16**. In this Figure, the oscillator is shown as a feedback system, generally referenced **230**. As described supra, a small input signal (V_i) e.g., noise, cannot remove the oscillator lock state at startup. Hence, a large disturbance on V_i is needed to pull the oscillator out of the lock state. Consider

a high swing sinusoidal signal on V_i. This signal can switch the first buffer in the loop on and off. Consequently, the output of the first stage can switch subsequent stages respectively. Finally, the output signal (V_o) is fed back to the input and causes further switching in the loop. At this time, the lock state is broken down and V_i can be removed. If the propagated disturbance signal in the loop can find enough gain, it builds up and the oscillation stabilizes.

A circuit diagram illustrating a seventh embodiment of the ring oscillator of the present invention incorporating a startup circuit that injects a short pulse to the oscillator loop is shown in FIG. 17A. A diagram illustrating example waveforms of the circuit of FIG. 17A is shown in FIG. 17B. In this circuit, generally referenced 240, a short input pulse can be injected to the loop to launch oscillation. The shape of the input pulse is optimized to find the input signal which creates the largest output amplitude on V_o at the end of the first cycle. For example, a one cycle sine wave signal with a period equal to the period of the oscillator can produce a higher amplitude than the same input with a (much) shorter period. The input disturbance signal with optimum shaping may not be practical to implement. A practical implementable signal shape is a single square pulse 242 which when injected into the loop results in V_1 244 shown in FIG. 17B.

First, consider lock state 1 in which M_{1p}, M_{2n}, M_{3p}, and M_{4n} are on and the other transistors are off. In lock state 2, M_{1n}, M_{2p}, M_{3n}, and M_{4p} are on and the other transistors are off. Connecting V_1 to ground by M_{sw1} causes two events to happen: (1) the input disturbance signal changes the state of V_{d2} and consequently a sinusoidal wave propagates through the loop; and (2) L_1 is charged through M_{sw1} and M_{1p} while V_4 is maintains its initial state. By releasing M_{sw1} the energy stored in L_1 is released and creates a new sine wave that propagates into the loop. To generate the largest injected wave in the loop (i.e. sinusoidal wave on V_1) which ensures more reliable startup, the two previously discussed waves should be in phase at V_1. This means that the first falling edge of V_{d1} coincides with the first peak of V_1 caused by releasing M_{sw1}. This can be achieved by the proper adjustment of t_p. The optimum value of t_p is between ¼ to ½ of the oscillation period, which can be determined from simulation, for example. For lock state 2, another switch (i.e. M_{sw2}) on V_2 is needed to inject the disturbance signal into the loop with the same procedure. Note that for the sake of simplicity we disregard lock state 2.

A circuit diagram illustrating an eighth embodiment of the ring oscillator of the present invention incorporating a startup circuit that includes an auxiliary oscillator is shown in FIG. 18A. A diagram illustrating example waveforms of the circuit of FIG. 18A is shown in FIG. 18B. In another circuit, generally referenced 250, an auxiliary oscillator 254 comprising inverters 262 is connected to one of the nodes in the feedback loop of the main oscillator for a short period of time, using a T-gate switch 252 comprising transistors 256, 258 and inverter gate 260 controlled by V_{ctrl}. If the auxiliary oscillator has sufficient driving strength, as well as an oscillation frequency almost the same as the main oscillator, it can launch oscillation of the main oscillator. Later, the auxiliary oscillator is disconnected and then turned off. In this manner, the power consumption overhead of the auxiliary oscillator is minimized. FIG. 18B shows the transient waveforms V_{ctrl} 264, Aux Osc 266 and V_1 268 of the startup circuit.

A circuit diagram illustrating a ninth embodiment of the ring oscillator of the present invention incorporating a startup circuit that includes back to back inverter pairs is shown in FIG. 19. The circuit, generally referenced 270,

comprises a two back to back inverter pairs 272. Each pair of back-to-back inverters 272 forces a 180 degree phase shift between V_{d1} and V_{d3} and between V_{d2} and V_{d4}. When these inverters are sized appropriately, the lock states are avoided and oscillation can be started easily. Note that these inverters having a small size can be combined with other start up circuits of FIGS. 17A and 18A as an additional aid to startup oscillation.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

The corresponding structures, materials, acts, and equivalents of all means or step plus function elements in the claims below are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The description of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the invention in the form disclosed. As numerous modifications and changes will readily occur to those skilled in the art, it is intended that the invention not be limited to the limited number of embodiments described herein. Accordingly, it will be appreciated that all suitable variations, modifications and equivalents may be resorted to, falling within the spirit and scope of the present invention. The embodiments were chosen and described in order to best explain the principles of the invention and the practical application, and to enable others of ordinary skill in the art to understand the invention for various embodiments with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. A ring oscillator, comprising:
a plurality of LC-tank based phase shifters configured in a loop;
a plurality of amplifiers, each amplifier coupled to and associated with one of said phase shifters;
wherein a gain of said plurality of amplifiers combined with voltage amplification of said phase shifters is sufficient to maintain oscillation in said loop; and
a startup circuit connected to a node in said loop and active for a finite period of time, said startup circuit operative to generate an initial oscillation in said loop.

2. The ring oscillator according to claim 1, wherein each phase shifter comprises a series inductor and capacitor.

3. The ring oscillator according to claim 2, wherein said inductor is coupled to an output of said amplifier while one terminal of said capacitor is coupled to ground.

4. The ring oscillator according to claim 3, wherein an output of each phase shifter comprises a node between said inductor and said capacitor.

5. The ring oscillator according to claim 1, wherein one or more of said amplifiers comprises an inverter.

6. The ring oscillator according to claim 1, wherein one or more of said amplifiers comprises a nonlinear amplifier.

7. The ring oscillator according to claim 1, wherein said startup circuit is operative to generate a single square pulse.

8. The ring oscillator according to claim **1**, wherein said startup circuit is turned off and disconnected after oscillation in said loop is established.

9. The ring oscillator according to claim **1**, wherein said startup circuit comprises back to back inverter pairs coupled to one or more nodes in said loop.

10. The ring oscillator according to claim **1**, further comprising a plurality of first tuning capacitors, each first tuning capacitor coupled to and associated with an input of one of said amplifiers and operative to provide relatively coarse frequency tuning control of said ring oscillator.

11. The ring oscillator according to claim **1**, further comprising a plurality of second tuning capacitors, each second tuning capacitor coupled to and associated with an output of one of said amplifiers and operative to provide relatively fine frequency tuning control of said ring oscillator.

12. A quadrature ring oscillator, comprising:

a plurality of four phase shifters, each of substantially 90 degrees, configured in a loop;

a plurality of four active circuits, each active circuit coupled in series with one of said phase shifters;

a plurality of tuning capacitors, each tuning capacitor coupled to and associated with one of said active circuits;

a startup circuit connected to one or more nodes in said loop and active for a finite period of time, said startup circuit operative to generate an initial oscillation in said loop;

wherein a gain of said plurality of active circuits combined with voltage amplification of said phase shifters is sufficient to maintain oscillation in said loop; and

wherein each active circuit is arranged in a single ended configuration.

13. The ring oscillator according to claim **12**, wherein the gain of said active circuits combined with voltage amplification of said phase shifters is sufficient to satisfy Barkhausen phase and gain criteria and cause said loop to oscillate.

14. The ring oscillator according to claim **12**, wherein each phase shifter comprises a series LC-tank.

15. The ring oscillator according to claim **12**, wherein said startup circuit comprises an auxiliary oscillator.

16. The ring oscillator according to claim **14**, wherein an inductor in said LC-tank is coupled to an output of said active circuit while one terminal of a capacitor in said LC-tank is coupled to ground.

17. The ring oscillator according to claim **16**, wherein an output of each phase shifter comprises a node between said inductor and said capacitor.

18. The ring oscillator according to claim **12**, wherein one or more of said active circuits comprises an inverter.

19. The ring oscillator according to claim **12**, wherein one or more of said active circuits comprises a nonlinear amplifier.

20. The ring oscillator according to claim **12**, wherein one or more of said active circuits comprises a buffer.

21. The ring oscillator according to claim **12**, wherein said startup circuit is operative to generate a single square pulse.

22. The ring oscillator according to claim **12**, wherein said startup circuit is disconnected after oscillation in said loop is established.

23. The ring oscillator according to claim **12**, wherein said startup circuit comprises back to back inverter pairs coupled to one or more nodes in said loop.

24. The ring oscillator according to claim **12**, wherein said tuning capacitors comprise first tuning capacitors, each first tuning capacitor coupled to an input of a respective active circuit and operative to provide relatively coarse frequency tuning control of said ring oscillator.

25. The ring oscillator according to claim **12**, wherein said tuning capacitors comprise second tuning capacitors, each second tuning capacitor coupled to an output of a respective active circuit and operative to provide relatively fine frequency tuning control of said ring oscillator.

26. The ring oscillator according to claim **12**, wherein said tuning capacitors comprise:

first tuning capacitors, each first tuning capacitor coupled to an input of a respective active circuit and operative to provide relatively coarse frequency tuning control of said ring oscillator; and

second tuning capacitors, each second tuning capacitor coupled to an output of a respective active circuit and operative to provide relatively fine frequency tuning control of said ring oscillator.

27. The ring oscillator according to claim **1**, wherein said startup circuit comprises an auxiliary oscillator.

28. The ring oscillator according to claim **1**, wherein said startup circuit is operative to inject one or more pulses into said loop.

29. The ring oscillator according to claim **12**, wherein said startup circuit is operative to inject one or more pulses into said loop.

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