A novel testing mechanism operative to test large capacitor arrays such as those used in a digitally controlled crystal oscillator (DCXO). The invention is adapted for use in DCXO circuits that employ dynamic element matching in their array decoding circuits. The invention combines the use of DEM during regular operation of the DCXO with a testing technique that greatly reduces the number of tests required. The invention tests the capacitors in the array on a row by row, wherein all the capacitors in a row are tested lumped together and treated as a single entity, which results in significantly reduced testing time. This permits the measurement of significantly higher frequency deviations due to the larger capacitances associated with an entire row of capacitors being tested.
OTHER PUBLICATIONS


**FIG. 1**
PRIOR ART

![Diagram showing an oscillator (Colpitts) with digital tuning and varactor/matrix connections.]

**FIG. 2**
PRIOR ART

![Graph showing frequency vs. code for prior art.]

- Oscillator (Colpitts)
- Digital tuning
- Varactor/matrix
- Frequency vs. code graph
FIG. 3

TEST MODE CONTROL

DIGITAL TUNING

TEST MODE/ NORMAL OPERATION

DCXO WITH DEM

ROW DECODE

COL DECODE

DYNAMIC ELEMENT MATCHING (DEM)

CAPACITOR MATRIX

OSCILLATOR

OSC OUTPUT
DCXO CAPACITOR MATRIX TEST METHOD

1. Initialize row = 1
2. Set all columns to "0"
3. Measure frequency
4. Oscillator output within specifications?
   a. Yes
      i. Set all columns to "1"
      ii. Measure frequency
      iii. Oscillator output within specifications?
         a. Yes
            i. Report defective row/matrix
            ii. End
         b. No
            i. Row = row + 1
            ii. Row > max rows?
               a. Yes
                  i. End
               b. No

FIG. 5
FIG. 6
BUILT-IN SELF TEST METHOD FOR A DIGITALLY CONTROLLED CRYSTAL OSCILLATOR

REFERENCE TO PRIORITY APPLICATION

This application claims priority under 35 U.S.C. § 119(e) to U.S. Provisional Application Ser. No. 60/728,402, filed Oct. 19, 2005, entitled "Built-in self test method for digitally controlled crystal oscillator (DCXO)," incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

The present invention relates to the field of communications and more particularly relates to a built-in self test method for a digitally controlled crystal oscillator (DCXO).

BACKGROUND OF THE INVENTION

Crystal oscillators are used as stable frequency sources in a wide range of applications including RF, digital circuits, etc. Crystal oscillators, which are comprised of a crystal generally manufactured from quartz and an active amplifier that provides a negative resistance to perpetuate the oscillation, are widely used because they provide a relatively accurate clock/frequency source. They typically provide a better long-term stability and more particularly relates to a built-in self test method for a digitally controlled crystal oscillator (DCXO).

SUMMARY OF THE INVENTION

The present invention overcomes the problems associated with the prior art by providing a testing mechanism operative to test large capacitor arrays such as those used in a digitally controlled crystal oscillator (DCXO). The invention is operative in DCXO circuits that employ dynamic element matching, which is a technique originally used in analog DAC circuit designs to linearize mismatch between fixed elements by rotating or shifting between the different elements thus smearing or averaging any differences between them over time.

The invention takes advantage of the use of the DEM technique during regular operation of the DCXO by combining it with a novel testing technique. Rather than test the capacitor array by measuring the frequency of each individual capacitor, the present invention is operative to measure the capacitors in the array on a row by row, wherein all the capacitors in a row are tested lumped together and treated as a single entity. Thus, each row is treated as one unit and not as individual capacitors.

Thus, the test method of the present invention is operative to test the entire capacitor matrix by testing each entire row as a single entity. Rather than test each individual capacitor in the matrix with its impractical long and costly testing time, the present invention permits significantly reduced test time. Depending on the size of the array, the use of the test method of the invention permits the capacitor array to be tested.
whereas without it, testing of the array could not be performed due to the length and cost of testing each individual capacitor.

This greatly reduces the requirements for testing. Instead of requiring a test of each individual capacitor, the invention permits complete testing of the entire array by testing each row as a single unit. A benefit of this is that rather than needing to test a very small value of capacitance for possibly seconds (i.e. less than 1 Hz), the invention requires testing of \( N \) times that value (where \( N \) is the number of capacitors in a row) which translates to a much higher and more practical frequency to measure since testing entire rows generates significantly higher frequency deviations.

There is also provided in accordance with the invention, a method of testing a capacitor matrix organized as a plurality of rows and columns, for use in a digitally controlled oscillator (DCO) incorporating dynamic element matching (DEM), the method comprising the steps of performing testing of the capacitor matrix on a row by row basis, wherein each entire row of capacitors is tested as a single entity and analyzing results of each test against expected frequency characteristics of an entire row of capacitors combined.

There is also provided in accordance with the invention, a built-in self test method of testing a digitally controlled crystal oscillator (DCXO) comprising a capacitor matrix organized as a plurality of rows and columns and incorporating dynamic element matching (DEM), the method comprising the steps of testing the capacitor matrix on a row by row basis, wherein each row of capacitors is tested as a single unit and indicating a test failure if the results of a row test is not within a predetermined specification.

There is further provided in accordance with the invention, a digitally controlled crystal oscillator (DCXO) comprising an oscillator circuit coupled to an external crystal, a capacitor matrix coupled to the oscillator circuit, a row decode circuit coupled to the capacitor matrix, wherein a digital tuning command applied to the row decode circuit and the column decode circuit determines an output frequency of the DCXO, a dynamic element matching (DEM) circuit coupled to the row decode circuit and wherein use of the DEM circuit permits testing of the capacitor matrix on a row by row basis such that each row of capacitors is tested as a single unit.

There is also provided in accordance with the invention, a method of testing a plurality of capacitors, for use in a digitally controlled oscillator (DCO) incorporating dynamic element matching (DEM), the method comprising the steps of performing testing of groups of the capacitors, wherein each group of capacitors is tested as a single entity and analyzing results of each test against expected frequency characteristics of an entire group of capacitors combined.

There is further provided in accordance with the invention, a method of testing a plurality of digitally-controlled conversion devices in a circuit incorporating dynamic element matching (DEM), the method comprising the steps of performing testing of groups of the digitally-controlled conversion devices, wherein each group of the digitally-controlled conversion devices is tested as a single entity and analyzing results of each test against expected characteristics of an entire group of digitally-controlled conversion devices combined.

Note that some aspects of the invention described herein may be constructed as software objects that are executed in embedded devices as firmware, software objects that are executed as part of a software application on either an embedded or non-embedded computer system such as a central processing unit (CPU), digital signal processor (DSP), microcomputer, minicomputer, microprocessor, etc. running a realtime operating system such as WinCE, Symbian, OSE, Embedded LINUX, etc. or non-real time operating system such as Windows, UNIX, LINUX, etc., or as soft core realized HDL circuits embodied in an Application Specific Integrated Circuit (ASIC) or Field Programmable Gate Array (FPGA), or as functionally equivalent discrete hardware components.

**BRIEF DESCRIPTION OF THE DRAWINGS**

The invention is herein described, by way of example only, with reference to the accompanying drawings, wherein:

FIG. 1 is a block diagram illustrating a prior art digitally controlled crystal oscillator (DCXO) incorporating a varactor matrix;

FIG. 2 is a graph illustrating the cumulative nonlinearity of the prior art DCXO circuit of FIG. 1;

FIG. 3 is a block diagram illustrating an example embodiment of the DCXO self test mechanism of the present invention incorporating dynamic element matching (DEM);

FIGS. 4A to 4I are diagrams illustrating the dynamic element matching via cyclic shifting within a row;

FIG. 5 is a flow diagram illustrating the DCXO capacitor matrix test method of the present invention; and

FIG. 6 is a block diagram illustrating a generalized DEM based DAC circuit incorporating a plurality of analog elements.

**DETAILED DESCRIPTION OF THE INVENTION**

**Notation Used Throughout**

The following notation is used throughout this document.

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>AFC</td>
<td>Automatic Frequency Control</td>
</tr>
<tr>
<td>ASIC</td>
<td>Application Specific Integrated Circuit</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital to Analog Converter</td>
</tr>
<tr>
<td>DCXO</td>
<td>Digitally Controlled Crystal Oscillator</td>
</tr>
<tr>
<td>DEM</td>
<td>Dynamic Element Matching</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processor</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>HDL</td>
<td>Hardware Description Language</td>
</tr>
<tr>
<td>NMOS</td>
<td>n-channel Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
</tbody>
</table>

**Capacitor Matrix Test Mechanism**

The present invention is a testing mechanism operative to test large capacitor arrays such as those used in a digitally controlled crystal oscillator (DCXO). The invention is adapted for use in DCXO circuits that employ dynamic element matching in their array decoding circuits. The invention combines the use of DEM during regular operation of the DCXO with a testing technique that greatly reduces the number of tests required. The invention tests the capacitors in the array on a row by row, wherein all the capacitors in a row are tested lumped together and treated as a single entity, which results in significantly reduced testing time. This permits the measurement of significantly higher frequency deviations due to the larger capacitances associated with an entire row of capacitors being tested. Note that throughout this document, the terms capacitor and varactor are generally intended to be
used interchangeably. It is not critical to the operation of the invention whether the DCXO capacitor arrays are implemented using capacitors or varactors.

A block diagram illustrating an example embodiment of the DCXO self test mechanism of the present invention incorporating dynamic element matching (DEM) is shown in FIG. 3. The DCXO circuit, generally referenced 40, comprises an external quartz crystal 42, oscillator circuit 44, capacitor circuit 52, column decode circuit 54 and dynamic element matching (DEM) circuit 56. Note that the description of the test mechanism of the invention is provided in the context of an example matrix comprising 1024 capacitors organized as 32 rows by 32 columns. It is not intended that the invention be limited to the examples presented herein as one skilled in the art can apply the principles of the present invention to matrices of any desired size. It should also be noted that the term “matrix” is only for ease of understanding and to better deal with large number of similar-size devices for the purpose of their addressing and encoding of the input word that controls 20 their configuration. It does not imply that the device layout structure be done in exact row and column arrangement. The layout structure could be linear, two-dimensional, three-dimensional or even irregular.

A hardware description language (HDL) based implementation of the DEM of FIG. 3 is provided below in Listing 1.

---

Listing 1: HDL version of DEM Circuit

```vhdl
-- Compute the required shift amount
begin
  if clrz = '0' then
    bubble_x <= "00000000";
  elsif clrz = '1' then
    if col_srst_t = '1' or mem_dem_t = '0' then
      bubble_x <= "00000000";
    else
      -- detect bubble
      bubble_x(1) <= rot_col(8) and (not rot_col(1));
      for i in 2 to 8 loop
        bubble_x(i) <= rot_col(i-1) and (not rot_col(i));
      end loop;
      end if;
  end if;
end process;
```

---

An assumption of the invention is that the DCXO employs dynamic element matching in the row decode circuit. For a given tuning code, the DEM is operative to cyclically shift between the columns of a row each clock cycle thus averaging all the capacitors in a row over time. Use of DEM in the DCXO provides a level of fault tolerance in that a failure of one or two (or more) capacitors does not detrimentally effect the operation of the oscillator. At some point, however, too many failed capacitors will cause the output of the oscillator to go out of spec.

Diagrams illustrating the dynamic element matching via cyclic shifting within a row are shown in FIGS. 4A to 4H. For clarity sake, a smaller 8x8 capacitor matrix is shown rather than a 32x32. A tuning code of 19 is input to the DCXO and in a cyclic manner from one clock cycle to the next. In FIG. 4A, the capacitors in the first three columns are turned on. In FIG. 4B, the capacitors in columns 2, 3, 4 are turned on. This continues in FIG. 4C (columns 3, 4, 5), FIG. 4D (columns 4, 5, 6), FIG. 4E (columns 5, 6, 7), FIG. 4F (columns 6, 7, 8), FIG. 4G (columns 1, 7, 8) and FIG. 4H (columns 1, 2, 8). Note that although only eight cyclic shifts are shown, other shift orders are possible as well. The operation of the DEM for other codes, 20, 21, etc. is similar.

Thus, if the code within a row is 2 (out of 8), for example. Using DEM, no capacitors in the row are specifically assigned to that code. Rather, the two capacitors are effectively distributed throughout the row. On the first clock cycle columns 1 and 2, on the second clock cycle columns 2 and 3, and so on with rotations (i.e. cyclic shifts) at each clock cycle. It is important to note that the total number of capacitors remaining the same for a given code but the actual capacitors are rotated each clock cycle. Each code does not have a fixed corresponding location in the array.

Thus, the code only represents the total number of capacitors in the ‘on’ state, which in this example is 8+8+3=19. This code corresponds to a certain frequency deviation. With every clock cycle the actual columns turned on within row three are cycled. In this example, after eight clock cycles, we return to the starting point. Consider that the capacitor in column one in the third row is defective. Therefore, in FIG. 4A, instead of generating a frequency corresponding to code 19, the DCXO
generates a frequency corresponding to code 18, since the first capacitor does not have an effect on the output. On the next clock cycle in FIG. 4B, however, the three capacitors exercised are all good. The effective code is therefore 19. In FIGS. 4C, 4D, 4E and 4F, the effective code is also 19. In FIGS. 4G and 4H, however, the effective code is 18.

When the DEM occurs quickly, the average value of the number of the effective code is between 18 and 19. Thus, the effect of the bad capacitor in significantly mitigated since what appears at the output of the oscillator is the averaged code value. Considering the 32×32 matrix, a failure of a single capacitor in a row only causes a loss of 1/32 in capacitance when the entire row is considered as a whole.

The invention takes advantage of the use of the DEM technique during regular operation of the DCXO by combining it with a novel testing technique as described hereinbelow. Rather than test the array of capacitors by measuring the frequency of each individual capacitor, the present invention is operative to measure the capacitors in the array on a row by row, wherein all the capacitors in a row are tested lumped together as a single entity. Thus, each row is treated as one unit and not as individual capacitors.

For example, the DCXO may be part of an automatic frequency control (AFC) algorithm. A digital tuning command (e.g., control word) 60 is provided which corresponds to some desired frequency change in the oscillator output. If the oscillator output does not change, the circuit the DCXO is part of is declared defective. Thus, the test mechanism of the invention is used to test the capacitor array. Although the size of the capacitors may be on order of femtofarads, corresponding to very small frequency deviations, when considering an entire row, the total capacitance is an order of magnitude higher with the consequence increase in frequency and decrease in required test time.

Thus, a key aspect of the invention is that each capacitor in the matrix is not tested individually. Rather, each row of 32 capacitors, in the example presented herein, is treated as a single unit without any loss of resolution since the DCXO applies DEM during operation. By using DEM during operation of the DCXO, there is now no need to test all the capacitors in the matrix (e.g., all 1024). It is sufficient to only test the rows as single entities. Thus, the complexity of the testing requirements is greatly reduced from 1024 individual capacitor tests to 32 row tests.

A benefit of this is that rather than needing to test a very small value of capacitance for possibly seconds (i.e. less than 1 Hz), the invention requires testing of 32 times that value which translates to a much higher and more practical frequency change to measure since testing entire rows generates significantly higher frequency deviations. Thus, use of the test mechanism of the invention replaces the need for 1024 impractically long and costly tests with 32 tests that can be performed practically using modern test equipment. Note that the invention assumes that the total number of defects per row is small, which is a valid assumption with modern semiconductor processing.

It should be noted that although there appears to be no benefit of DEM when the entire row is filled, there are many possible sequences of rotation which guarantee a certain amount of empty cells in a row or multiple rows. In addition, a combination of row and column rotation could be used to implement DEM.

A flow diagram illustrating the DCXO capacitor matrix test method of the present invention is shown in FIG. 5. This method can be used by external test equipment during the manufacturing process or can be implemented internally by built-in self test circuitry within the IC incorporating the DCXO of the present invention. In addition, portions of the method may be implemented in both external test equipment and on the IC itself.

An example of such a built-in self test is described in a U.S. Pub. No. 2004/0146132 A1, published Jul. 29, 2004, to Staszewski et al., entitled "Radio Frequency Built-In Self Test For Quality Monitoring Of Local Oscillator And Transmitter," incorporated herein by reference in its entirety. The digital phase detector output signal (or its filtered version) is monitored and the frequency change of the frequency reference (FREF) input, which is connected to the DCXO output, is calculated. This method relies on the following principles that tie the internal ADPLL signals to the frequency change on its reference input: (1) in type-I PLLs, in which the integral part of the loop filter is not used, the difference between the steady-state average or filtered values of the phase error is proportional to the reference frequency step; (2) in type-II PLLs, in which the integral part of the loop filter is non-zero, the steady state change in the “rho” or integral accumulator is proportional to the reference frequency step.

The method steps through the rows one by one and performs tests on each row as a whole. The method first initializes a row variable to one (step 60). Capacitors in every column of the row are then configured to the digital ‘0’ state (step 64). The resultant frequency is then measured (step 66). The digital ‘0’ state of all capacitors ‘off’ should yield a known output from the oscillator. If the oscillator output does not meet the given specifications (step 68), an alarm or report indicating a defective row (or matrix in general) is generated (step 80).

If the oscillator output does meet the given specifications (step 68), all columns in the row are then configured to the digital ‘1’ state (step 70) and the resultant oscillator output frequency is measured (step 72). If the oscillator output does not meet the particular specification (step 74), an alarm or report indicating a defective row (or matrix in general) is generated (step 80). If the oscillator output does meet the given specifications (step 74), the row variable is incremented by one (step 76) and if there are additional rows to test (step 78), the method continues with step 64. Thus, the frequency step from all 0s to all is measured.

Thus, the test method of the present invention is operative to test the entire capacitor matrix by testing each entire row as a single entity. Rather than test each individual capacitor in the matrix with its impractical long and costly test time, the present invention permits significantly reduced test time. Depending on the size of the array, the use of the test method of the invention permits the capacitor array to be tested whereas without it, testing of the array could not be performed due to the length and cost of testing each individual capacitor.

It is noted that it is the use of the DEM circuit in the DCXO that permits the testing of the array on a row by row basis. The cyclic shifting of capacitors by the DEM eliminates the one to one relationship between each code and the capacitors that are turned on in response thereto. Thus, failures of individual capacitors within a row (up to a certain number) are averaged thereby providing a level of fault tolerance for the DCXO. This aspect of the operation of the DEM permits the testing of the array on a row by row basis since individual failed capacitors do not necessarily result in the declaration of a failed array.

It should be noted that the methods and techniques presented herein apply to a general class of digitally-controlled oscillators (DCOs), in which the resonating device may comprise not only a crystal, but an LC tank, inverter ring, microwave guide, etc. Furthermore, the present invention of capaci-
In addition to testing capacitances, the testing mechanism of the present invention can be applied to other electrical elements as well, such as resistors, inductors or even gain elements.

A block diagram illustrating a generalized DEM based circuit incorporating a plurality of analog elements (or digitally-controlled conversion devices). The circuit, generally referenced 90, comprises a unit weighted encoder and DEM block 92 and a conversion cell block 94 comprising a plurality of analog cells 96. In a general case of a digital-to-analog converter (DAC), where the 'A' in DAC denotes 'analog' which may comprise any analog quantity (e.g., voltage, current, resistance, capacitance, frequency, power, etc), the digitally-controlled conversion devices could also be arranged using similar philosophy of using an extremely large number of the tiny unit-weighted devices.

Since it would be equally difficult to measure the tiny conversion gain of each individual device for the purpose of fault testing, the devices could be arranged such that a set of the devices would be undergoing periodical but frequent rotation as controlled by the DEM circuit. In this manner, a fault of one or a small number of devices are averaged out with good devices in order to minimize the effect of the fault. In the case of the embodiments described supra, the analog quantity ('A' in DAC) is capacitance, which gets further converted into frequency deviation through the LC resonating tank-based oscillator.

In alternative embodiments, the methods of the present invention may be applicable to implementations of the invention in integrated circuits, field programmable gate arrays (FPGAs), chip sets or application specific integrated circuits (ASICs), DSP circuits, wired or wireless implementations and other communication system products.

It is intended that the appended claims cover all such features and advantages of the invention that fall within the spirit and scope of the present invention. As numerous modifications and changes will readily occur to those skilled in the art, it is intended that the invention not be limited to the limited number of embodiments described herein. Accordingly, it will be appreciated that all suitable variations, modifications and equivalents may be resorted to, falling within the spirit and scope of the present invention.

What is claimed is:

1. A method of testing a capacitor matrix organized as a plurality of rows and columns, for use in a digitally controlled oscillator (DCO) incorporating dynamic element matching (DEM), said method comprising the steps of:
   - performing testing of said capacitor matrix on a row by row basis, wherein each entire row of capacitors is tested as a single entity; and
   - analyzing results of each test against expected frequency characteristics of an entire row of capacitors combined.
2. The method according to claim 1, wherein testing entire rows of capacitors as a single entity results in a significantly higher expected oscillator frequencies than compared with testing individual capacitors.
3. The method according to claim 1, wherein said step of performing testing comprises the step of setting all capacitors in a row to an 'on' state and measuring the resultant oscillator output frequency.
4. The method according to claim 1, wherein said step of performing testing comprises the step of setting all capacitors in a row to an 'on' state and measuring the resultant oscillator output frequency.
5. The method according to claim 1, wherein said capacitor matrix is organized as 32 rows by 32 columns.
6. A built-in self test method of testing a digitally controlled crystal oscillator (DCXO) comprising a capacitor matrix organized as a plurality of rows and columns and incorporating dynamic element matching (DEM), said method comprising the steps of:
   - testing said capacitor matrix on a row by row basis, wherein each row of capacitors is tested as a single unit; and
   - indicating a test failure if the results of a row test is not with a predetermined specification.
7. The method according to claim 6, wherein said step of testing comprises the step of setting all capacitors in a row to an 'on' state and measuring the resultant oscillator output frequency.
8. The method according to claim 6, wherein said step of testing comprises the step of setting all capacitors in a row to an 'on' state and measuring the resultant oscillator output frequency.
9. The method according to claim 6, wherein said capacitor matrix is organized as 32 rows by 32 columns.
10. The method according to claim 6, wherein said step of indicating a test failure comprises analyzing the results of each test against expected frequency characteristics of an entire row of capacitors combined.
11. The method according to claim 6, wherein use of said DEM circuit permits testing of said capacitor matrix on a row by row basis such that each row of capacitors is tested as a single unit.
12. The method according to claim 6, wherein said DEM provides a degree of tolerance against a certain number of failed capacitors within each row of said matrix.
13. A digitally controlled crystal oscillator (DCXO), comprising:
   - an oscillator circuit coupled to an external crystal;
   - a capacitor matrix coupled to said oscillator circuit;
   - a row decode circuit coupled to said capacitor matrix;
   - a column decode circuit coupled to said capacitor matrix, wherein a digital tuning command applied to said row decode circuit and said column decode circuit determines an output frequency of said DCXO;
   - a dynamic element matching (DEM) circuit coupled to said row decode circuit; and
   - wherein use of said DEM circuit permits testing of said capacitor matrix on a row by row basis such that each row of capacitors is tested as a single unit.
14. The apparatus according to claim 13, wherein said DEM circuit is operative to provide a level of fault tolerance to said DCXO through cyclic shifting of columns within each row.
15. The apparatus according to claim 13, wherein said DEM circuit is operative to average the effect of failed capacitors in a row thus enabling the testing of said capacitor matrix on a row by row basis.
16. The apparatus according to claim 13, wherein testing entire rows of capacitors as a single entity enables testing for significantly higher expected oscillator output frequencies than compared with individual capacitors.
17. The apparatus according to claim 13, wherein testing comprises setting all capacitors in a row to an 'off' state and measuring the resultant oscillator output frequency.
23. A method of testing a plurality of digitally-controlled conversion devices in a circuit incorporating dynamic element matching (DEM), said method comprising the steps of:

- performing testing of groups of said digitally-controlled conversion devices, wherein each group of said digitally-controlled conversion devices is tested as a single entity;
- analyzing results of each test against expected frequency characteristics of an entire group of digitally-controlled conversion devices combined.

24. The method according to claim 23, wherein said digitally-controlled conversion devices comprise varactors.

25. The method according to claim 23, wherein said analyzing means are based on monitoring a phase error signal.

18. The apparatus according to claim 13, wherein testing comprises setting all capacitors in a row to an 'on' state and measuring the resultant oscillator output frequency.

19. The apparatus according to claim 13, wherein said capacitor matrix is organized as 32 rows by 32 columns.

20. The apparatus according to claim 13, further comprising means for determining a change to said DCXO frequency based on monitoring of a phase error signal.

21. The apparatus according to claim 13, further comprising means for determining a change to said DCXO frequency based on monitoring of accumulated phase error.

22. A method of testing a plurality of capacitors, for use in a digitally controlled oscillator (DCO) incorporating dynamic element matching (DEM), said method comprising the steps of:

- performing testing of groups of said capacitors, wherein each group of capacitors is tested as a single entity; and
- analyzing results of each test against expected frequency characteristics of an entire group of capacitors combined.

23. A method of testing a plurality of digitally-controlled conversion devices in a circuit incorporating dynamic element matching (DEM), said method comprising the steps of:

- performing testing of groups of said digitally-controlled conversion devices, wherein each group of said digitally-controlled conversion devices is tested as a single entity;
- and
- analyzing results of each test against expected characteristics of an entire group of digitally-controlled conversion devices combined.

24. The method according to claim 23, wherein said digitally-controlled conversion devices comprise varactors.

25. The method according to claim 23, wherein said analyzing means are based on monitoring a phase error signal.