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Microwave-compatible digital phase lock loop architecture

Abstract

A novel and unique apparatus for and method of activity based phase locked loop (PLL) is disclosed. The apparatus incorporates microprocessor and digital circuitry to provide a microwave-compatible phase locked loop (PLL) with a wide range of output frequencies. The apparatus and method of the present invention provides a microprocessor (MP) incorporating the PLL circuitry on monolithic or hybrid substrate, or alternatively, a microprocessor is optimized to perform the operation of PLL. The PLL is clocked at a fast enough rate to provide a wide range of output frequencies, and to provide a microwave-compatible phase locked loop.

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In contrast, the mechanism of the present invention is operative to perform the atomic operations serially at the much faster processor rate. At each processor cycle, only a single instruction is executed resulting in reduced current transients being generated, as indicated in trace 376. This results in significantly reduced RF spur generation. In the present invention, the effects these generated spurs have on RF performance are two-fold: (1) the spurs are shifted to higher frequencies where they are easier to filter out by the oscillator's LC tank, DPA matching network, PA matching network, bandpass filtering in the RF front-end module, as well as overall parasitic RC (resistor-capacitor) network; and (2) the energy of each spur is reduced.

In accordance with the invention, the software based ADPLL significantly reduces the generation of RF spurs in sensitive frequency bands of the DRP by changing the frequency plan of the switching logic gates. The ASIP/RCU performs the bulk of computations at the processor clock rate which is much higher in frequency than that of the system reference clock (FREF). This result in the RF spurs being shifted outside the sensitive regions close to the carrier frequency as shown in FIG. 22. The processing clock spurs 392 are now far away from the carrier 392 and the filtering envelope 390 is able to remove these spurs with ease.

It is noted that the total amount of energy consumed in performing computations in the conventional ADPLL and the software based ADPLL of the invention is substantially the same. The frequency content of this energy, however, is significantly different. In case of the conventional ADPLL, the computation energy is concentrated at the reference clock edges and therefore has strong low frequency harmonic.

In case of the software based ADPLL, the computation energy is spread out between the reference clock edges (which may or may not coincide with the processor clock edges). The spreading out of the computation energy over the reference clock period serves to create a much higher frequency harmonic. When these harmonics mix with the carrier, they are offset in frequency around the carrier. The filtering requirements to remove the undesired RF spurs close to the carrier are excessive, as in the case of the conventional ADPLL. The further away from the carrier the RF spurs are located, the more relaxed the filtering requirements become. Changing the frequency content of the computation energy to improve the RF spectrum characteristics is referred to as frequency planning. Such frequency planning also helps to relax circuit design constraints, such as power routing resistance and decoupling capacitance values, which contribute to the magnitude of the energy surges at the clock edges.

Further, the frequency planning can be modified by varying the amount of oversampling (i.e. the ratio of processor clock frequency to the reference frequency FREF). The frequency planning can be lowered as long as the minimum required processing throughput in the processor is maintained. Otherwise, the required atomic operations of the ADPLL may not be completed within a reference clock cycle.

It is appreciated that the application of the software based mechanism described herein is not limited to an ADPLL. The mechanism can be applied to any computing or processing task that can benefit from reduced spur generation. A flow diagram illustrating the RF spur reduction method of the present invention is shown in FIG. 23. In the general case, the task is first partitioned into a plurality of atomic operations (step 740). The computation of the atomic operations required to complete the task are spread out over an entire reference clock period (step 742). The computation of each atomic operation occurs at the higher processor clock rate, rather that the slower reference clock rate (step 744).

Several embodiments of the processor based mechanism will now be presented. Each is an alternative implementation of the software based ADPLL. A block diagram illustrating an example ASIP based implementation of the software ADPLL of the present invention is shown in FIG. 24. The software based ADPLL, generally referenced 550, comprises a phase domain calculator 552, DCO 556, programmable fractional-N clock divider 554, integer feedback block 578 and fractional feedback block 579. The phase domain calculator 552 comprises an ALU (RCU) 572, instruction and data memory 558, register file 560, sequencer 562, latches 566, 576, multiplexers 564, 568, 570, 574.

A block diagram illustrating an example DSP based implementation of the software ADPLL of the present invention is shown in FIG. 25. The software based ADPLL, generally referenced 580, comprises a phase domain calculator 582, DCO 586, programmable fractional-N clock divider 584, integer feedback block 588 and fractional feedback block 590. The phase domain calculator 582 comprises memory block (RAM/ROM) 594, a DSP core 595, external bus interface (I/F) 592, UART 596 and timer 598.

A block diagram illustrating an example hardware state machine based implementation of the software ADPLL of the present invention is shown in FIG. 26. The software based ADPLL, generally referenced 600, comprises a phase domain calculator 602, DCO 606, programmable fractional-N clock divider 604, integer feedback block 608 and fractional feedback block 610. The phase domain calculator 602 is similar in construction and operation to the phase calculation 222 (FIG. 10). In particular, the phase domain calculator 602 comprises flip-flops 612, 616, 624, 630, 634, 656, 650, 638, subtractors 614, 654, adder 628, multipliers 622, 632, 652, accumulators 618, 658, differentiator 636, IIR bocks 620, 626, Lamba register 640, PHE offset register 642, Gain1 register 646, Gain2 register 648 and Gain3 register 644.

A block diagram illustrating a first example implementation of the state machine used to implement the software ADPLL of the present invention is shown in FIG. 27. The circuit, generally referenced 660, comprises a clock generator circuit 662 and a plurality of finite state machines (FSMs) 664, 666, 668, 670. The clock generator is operative to generate the clock signals for the functional units, i.e. FSM1, FSM2, FSM3, FSM4. Although only four units are shown for the sake of simplicity, it is appreciated that any number of state machines may be implemented.

The functional units are executed in a sequential manner to provide the desired overall functionality of a subsystem such as a PLL or other circuit/task. An input of a functional unit is connected to the output of the previous unit with the last unit feeding the first unit. Only a simple circular arrangement is shown although the technique is applicable to more complicated arrangements as well, such as forking and merging.

The higher frequency clock CKVD 672 is generated by performing frequency or edge division of the variable clock CKV. The CKVD clock is used to generate internal clocks CK1, CK2, CK3, CK4, each one providing significant edges to its respective functional units FSM1, FSM2, FSM3, FSM4. The frequency of the CKVD clock is chosen so as to guarantee that all the elementary functional operations performed by functional units FSM1, FSM2, FSM3, FSM4 are executed within a single reference clock FREF cycle 674. This is accomplished by requiring the CKVD clock to be (in this example) at least four times faster (i.e. the number of functional units) than the FREF clock. In the example presented in FIG. 27, the frequency ratio is approximately 4.6.

A block diagram illustrating a second example implementation of the state machine used to implement the software ADPLL of the present invention is shown in FIG. 28. The circuit, generally referenced 680, comprises clock and phase generator 682 and FSM 684. This figure presents the embodiment wherein the functionality of the various functional units (i.e. FSM1, FSM2, FSM3, FSM4) are merged into a single reconfigurable finite state machine (FSM). The FSM unit reprograms itself such that its functionality becomes one of the four units FSM1, FSM2, FSM3, FSM4 of FIG. 27. The determination of which unit the FSM 684 becomes is controlled by the "Phase" signal. The input and output connections between the functional units in FIG. 27 are now stored as state variables internal to the FSM, which now operates at a higher clock rate 688. The single clock line CK comprises gaps due to the non-integer frequency ratio of CKVD to FREF 689.

It is intended that the appended claims cover all such features and advantages of the invention that fall within the spirit and scope of the present invention. As numerous modifications and changes will readily occur to those skilled in the art, it is intended that the invention not be limited to the limited number of embodiments described herein. Accordingly, it will be appreciated that all suitable variations, modifications and equivalents may be resorted to, falling within the spirit and scope of the present invention.

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