A buffering circuit for buffering an oscillator signal. The buffering circuit includes a plurality of PMOS and NMOS transistor pairs connected in parallel, each pair having connected gate terminals and connected drain terminals forming an inverter circuit, each pair arranged for receiving via a direct coupling an oscillator signal at its gate terminal, and each pair further being connected with an additional PMOS and NMOS transistor. The buffering circuit also includes a control circuit arranged for receiving an output signal provided by the inverter circuits, for deriving information on the DC level of the output signal, and for adjusting a voltage transfer curve expressing a relationship between a voltage at the input and output of the buffering circuit, by switching on or off the additional PMOS and NMOS transistors based on the derived information.
Corner: fast-fast

Corner: slow-slow
The oscillator is not incorporated in a PLL and operates in power amplifier or divider circuits that warrant rail-rail swings much lower than the rail-to-rail level (i.e. VDD to GND). The oscillator buffer thus also serves to drive the power amplifier (PA) or divider blocks directly by the oscillator. In other words, the DC level of the oscillator is not ensured to lie at the intersection of the VTC and the DC level of the oscillator output is prone to process, voltage and temperature variations, this DC level may vary. Conventionally, a self-biased inverter is used as an oscillator buffer, which is AC-coupled to the oscillator output by means of a large coupling capacitor \( C_{OUT} \). Fig. 3 provides an illustration. AC-coupling indicates that only an AC signal results in an output signal with a 50% duty cycle for a sinusoidal input; any voltage greater than this bias voltage gives a low output and vice versa. As the DC level of the oscillator output is prone to process, voltage and temperature variations, this DC level may vary. Conventionally, a self-biased inverter is used as an oscillator buffer, which is AC-coupled to the oscillator output by means of a large coupling capacitor \( C_{OUT} \). Fig. 3 provides an illustration. AC-coupling indicates that only an AC signal results in an output signal with a 50% duty cycle for a sinusoidal input; any voltage greater than this bias voltage gives a low output and vice versa.
more current to maintain the required phase noise levels. Furthermore, the large decoupling capacitor introduces significant parasitics, thereby loading the output node of the oscillator. This increases the power consumption and reduces the maximum operable frequency of the oscillator. Thus a self-biased inverter used as a buffering circuit poses a serious challenge in scaling down the power consumption and area. [0011] In the paper “A 915 MHz, Ultra-Low Power 2-Tone Transceiver With Enhanced Interference Resilience” (X. Huang et al., IEEE Journal Solid State Circuits, vol. 47, no. 12, December 2012, pp. 3197-3207) an AC-coupled LO buffer is used to isolate the low-swing oscillator from the power amplifier. It uses passive components and hence does not scale with technology. Also, it needs additional biasing, adding to the total power consumption.

[0012] Consequently, there is a need for an oscillator buffer wherein the above-mentioned drawbacks of the prior art solutions are avoided or overcome.

SUMMARY

[0013] It is an object of embodiments of the present disclosure to provide for an inverter based oscillator buffer wherein the use of passive components is avoided. It is a further object to provide a method for calibrating the oscillator buffer. [0014] The above objective is accomplished by the solution according to the present disclosure. [0015] A first aspect the disclosure relates to a buffering circuit for buffering an oscillator signal, the buffering circuit including a plurality of PMOS and NMOS transistor pairs connected in parallel, each pair having connected gate terminals and connected drain terminals forming an inverter circuit, each pair arranged for receiving via a direct coupling a sinusoidal oscillator signal with a variable DC level at its gate terminal, and each pair further being connected with an additional PMOS and NMOS transistor. The buffering circuit further includes a control circuit arranged for receiving an output signal output by the inverter circuits, and for deriving information on the DC level of the output signal, and for adjusting a voltage transfer curve expressing a relationship between a voltage at the input and output of the buffering circuit to match the variable DC level, by switching on or off the additional PMOS and NMOS transistors based on the derived information.

[0016] The proposed solution indeed allows for avoiding passive components. A DC coupling between the oscillator and the buffering circuit is possible. Variations in the DC level can be dealt with by providing a control circuit that receives at its input the buffer output signal and determines an indication of its DC level. Next the voltage transfer curve at the buffer input can be adjusted by appropriately switching the additional transistors in the circuit such that the DC-level at the buffer input and the maximum sensitivity point on the VTC are at the same voltage level.

[0017] In an embodiment the control circuit is arranged for deriving the information on the DC level by averaging the output signal.

[0018] In an embodiment the inverter circuit is implemented in CMOS.

[0019] In a potentially advantageous embodiment the transistor pairs of the plurality are sized such that they form binary weights. The gate widths of transistors belonging to different pairs then have a ratio that is a power of 2.

[0020] In another embodiment, the control circuit is arranged for adjusting the voltage transfer curve of the inverter circuit by generating code words and hence its output DC-level.

[0021] The disclosure also relates to a device comprising an oscillator and a buffering circuit as previously described.

[0022] Potentially advantageously, the oscillator is a voltage controlled oscillator or a digitally controlled oscillator.

[0023] In one embodiment the device comprises a further buffer arranged for receiving the output signal of the preceding buffer circuit. This is especially useful when a large load is applied, as it allows reducing the size of the preceding buffer circuit.

[0024] In an embodiment the oscillator of the device is part of a phase-locked loop.

[0025] In another aspect, the disclosure relates to a method for calibrating a buffering circuit, comprising applying via a direct coupling a sinusoidal oscillator signal with variable DC level to a circuit comprising a plurality of PMOS and NMOS transistor pairs connected in parallel, each pair having connected gate terminals and connected drain terminals forming an inverter circuit, each pair arranged for receiving the oscillator signal at its gate terminal, and each pair further being connected with an additional PMOS and NMOS transistor. The method also includes deriving information on the DC level of an output signal output by the inverter circuits, and adjusting a voltage transfer curve expressing a relationship between a voltage at the input and output of the buffering circuit to match the variable DC level, by switching on or off the additional PMOS and NMOS transistors based on the derived information.

[0026] For purposes of summarizing the disclosure and the advantages achieved over the prior art, certain objects and advantages of the disclosure have been described herein above. Of course, it is to be understood that not necessarily all such objects or advantages may be achieved in accordance with any particular embodiment of the disclosure. Thus, for example, those skilled in the art will recognize that the disclosure may be embodied or carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other objects or advantages as may be taught or suggested herein.

[0027] The above and other aspects of the disclosure will be apparent from and elucidated with reference to the embodiment(s) described hereinafter.

DESCRIPTION OF THE DRAWINGS

[0028] The present disclosure will now be described further, by way of example, with reference to the accompanying drawings, wherein like reference numerals refer to like elements in the various figures.

[0029] FIG. 1 illustrates a conventional scheme wherein the oscillator of a PLL and a load are isolated by a buffer.

[0030] FIG. 2 illustrates the determination of the maximum sensitivity point on a Voltage Transfer Curve (VTC).

[0031] FIG. 3 illustrates a conventional self-biased inverter scheme.

[0032] FIG. 4 illustrates the operational principle of a VTC tunable buffer according to the present disclosure.

[0033] FIG. 5 illustrates the shifting of the Voltage Transfer Curve.

[0034] FIG. 6 illustrates an embodiment of the buffer circuit according to the present disclosure.
[0035] FIG. 7 illustrates another embodiment of the buffer circuit according to the present disclosure.

[0036] FIG. 8 illustrates a detailed view on yet another embodiment of the buffer circuit according to the present disclosure.

[0037] FIGS. 9A-9C illustrate some simulation results of the proposed buffer circuit across a typical process corner, a fast process corner, and a slow process corner, respectively.

DETAILED DESCRIPTION

[0038] The present disclosure will be described with respect to particular embodiments and with reference to certain drawings but the disclosure is not limited thereto but only by the claims.

[0039] Furthermore, the terms first, second and the like in the description and in the claims, are used for distinguishing between similar elements and not necessarily for describing a sequence, either temporally, spatially, in ranking or in any other manner. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the disclosure described herein are capable of operation in other sequences than described or illustrated herein.

[0040] It is to be noticed that the term “comprising”, used in the claims, should not be interpreted as being restricted to the means listed thereafter; it does not exclude other elements or steps. It is thus to be interpreted as specifying the presence of the stated features, integers, steps or components as referred to, but does not preclude the presence or addition of one or more other features, integers, steps or components, or groups thereof. Thus, the scope of the expression “a device comprising means A and B” should not be limited to devices consisting only of components A and B. It means that with respect to the present disclosure, the only relevant components of the device are A and B.

[0041] Reference throughout this specification to “one embodiment” or “an embodiment” means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present disclosure. Thus, appearances of the phrases “in one embodiment” or “in an embodiment” in various places throughout this specification are not necessarily all referring to the same embodiment, but may. Furthermore, the particular features, structures or characteristics may be combined in any suitable manner, as would be apparent to one of ordinary skill in the art from this disclosure, in one or more embodiments.

[0042] Similarly it should be appreciated that in the description of exemplary embodiments of the disclosure, various features of the disclosure are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed disclosure require more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims following the detailed description are hereby expressly incorporated into this detailed description, with each claim standing on its own as a separate embodiment of this disclosure.

[0043] Furthermore, while some embodiments described herein include some but not other features included in other embodiments, combinations of features of different embodiments are meant to be within the scope of the disclosure, and form different embodiments, as would be understood by those in the art. For example, in the following claims, any of the claimed embodiments can be used in any combination.

[0044] It should be noted that the use of particular terminology when describing certain features or aspects of the disclosure should not be taken to imply that the terminology is being re-defined herein to be restricted to include any specific characteristics of the features or aspects of the disclosure with which that terminology is associated.

[0045] In the description provided herein, numerous specific details are set forth. However, it is understood that embodiments of the disclosure may be practiced without these specific details. In other instances, well-known methods, structures and techniques have not been shown in detail in order not to obscure an understanding of this description.

[0046] Hereto, in the context of the present disclosure an AC coupled circuit refers to a circuit with the output of a preceding circuit connected to a succeeding circuit by means of a decoupling capacitor, thereby blocking the DC signal while allowing the AC signal to pass through. A DC coupled circuit refers to a circuit where two consecutive circuits are connected directly without any decoupling capacitor, thereby allowing both AC and DC signals to pass through.

[0047] Also in the context of the present disclosure, a DC level of a sinusoidal signal refers to the average value of the signal in one cycle. Stated otherwise, it is the level about which the sinusoidal wave oscillates.

[0048] In the present disclosure bulky passive components are avoided by providing a DC coupling of the oscillator output to the buffer. Depending on the input DC level (DC level of the sinusoidal signal from the oscillator), the VTC of the buffer is shifted to ensure operation at maximum sensitivity across process, voltage and temperature (PVT) variations. The oscillator used in this disclosure can be e.g. a Voltage Controlled Oscillator (VCO), a Digitally Controlled Oscillator (DCO) or an oscillator operating in an open loop configuration. Advantageously the oscillator may be part of a PLL.

[0049] In the proposed solution decoupling the capacitor C_{bias} and the biasing resistor R_{bias} is avoided and the oscillator output is connected directly to the buffer. Consequently, the variation in the DC level of the oscillator output affects the operation of the buffer. Thus, to ensure the oscillator buffer always operates at its maximum sensitivity point, it is proposed to shift its VTC so that the DC level of the oscillator output corresponds to the maximum sensitivity point of the buffer. A more detailed explanation is provided below.

[0050] As explained previously, operation at the maximum sensitivity point V_{in} of the inverter results in the maximum possible gain. Thus, a low-swing input signal can be boosted to rail-to-rail levels, i.e. VDD to GND. Operating at the maximum sensitivity point of the buffer also results in a buffer output with 50% duty cycle for a sinusoidal input, as the input sinusoidal signal has equal duration for voltages above and below its DC level, hence the output signal also has a 50% duty cycle. However, any input voltage V_{in} greater than or lower than the input voltage value corresponding to maximum sensitivity point V_{in} results in an output voltage V_{out} with (i) a low swing (amplitude) and (ii) a lower or a higher duty cycle, as the inverter does not operate in its linear region. The duty cycle of the output voltage will increase or decrease
depending on whether the input DC level is smaller than or greater than the voltage corresponding to the maximum sensitivity point \( V_{n} \). For example, a very low output swing is observed for input voltage \( V_{n} \) having an average value close to zero or VDD. In case the DC-level of \( V_{n} \) is close to VDD, the duty cycle of the output voltage is small, nearly 0. Similarly, if the DC-level of \( V_{n} \) is close to zero, the duty cycle of the output voltage is nearly 100%. The information on the duty cycle of the buffer output voltage is used for calibrating (shifting) the buffer’s VTC along the X-axis to the desired position across PVT variations, ensuring compensation for any variations in the input DC level of the buffer. Any calibration circuit that can monitor and detect deviation in a duty cycle of a signal may be used for this purpose.

In the solution of the present disclosure a DC-coupled oscillator buffer is presented. The DC level at the buffer input is determined by the oscillator’s output DC level. The oscillator can be, for example, a voltage controlled oscillator (VCO) or a digitally controlled oscillator (DCO). The buffer’s VTC is shifted along the X-axis to ensure its maximum sensitivity point tracks the DC level of the oscillator output, which changes due to process, voltage and temperature variations. The disclosure further presents a technique for tuning the DC-coupled oscillator buffer. A feedback loop is provided comprising a control circuit adapted for adjusting the DC level of the buffer output by changing the voltage transfer curve of the buffer. Thus, the proposed solution aims at tuning the VTC of the inverter to match the maximum sensitivity point with the DC level of the VCO/DCO output.

Fig. 4 shows a block scheme of a device comprising an embodiment of the oscillator buffer according to the present disclosure. The device 10 comprises an oscillator 1, the output of which is directly connected to the input of buffer 21. The buffer may be implemented as a CMOS inverter. The buffer output is in the embodiment of Fig. 4 applied to an optional further buffer 22, which subsequently feeds its output to the power amplifier 3. Providing this additional buffer is beneficial in that it allows reducing the size of the first buffer when a large load needs to be driven.

A control circuit 4 is provided for shifting the buffer VTC to the required level. One possible way to realize this shift can be to detect the duty cycle of the buffer output by averaging the waveform to obtain the DC level. If for example the output voltage has an average value (i.e. DC level) greater than VDD/2, this indicates that its duty cycle is greater than 50% (the duration of the positive waveform is longer than the negative waveform). This translates to an input DC level lower than the input voltage corresponding to the maximum sensitivity point \( V_{n} \) of the buffer. Hence, the control circuitry turns on more NMOS transistors to shift the VTC to the left, so that a 50% duty cycle of \( V_{n} \) is achieved (i.e. the output voltage has an average value equal to VDD/2). Similarly, if the average is less than VDD/2, more PMOS transistors are enabled to ensure an output voltage \( V_{n} \) with 50% duty cycle.

Fig. 5 illustrates the VTC shifting for low-input swing operation of the buffer in order to track the input DC level across process variations. The VTC can be shifted by varying the overall ratio of the gate width of PMOS and NMOS transistors that form the buffer. The overall transistor ratio, denoted as \( W_{P}/W_{N} \), represents the total ratio of the sizes (or gate widths) of the PMOS and NMOS transistors forming the buffer. It is to be noted that since the transistor pairs are connected in parallel the sizes (gate widths) can simply be added. To this end, a set of complementary transistors (PMOS-NMOS) are connected in parallel to act as an inverter as shown in Fig. 6. Each respective transistor of the complementary set is connected to supply rails, i.e. PMOS to VDD and NMOS to GND, via an additional PMOS and an additional NMOS transistor, respectively. Depending on the state of the additional transistor (on or off), the respective transistor of the complementary set is connected to VDD or GND. Thus, the additional transistors act as switches to connect or disconnect their respective transistor of the set of complementary transistors to VDD or GND, resulting in a change of the overall \( W_{P}/W_{N} \) ratio of the buffer and hence a shift of its VTC. The PMOS and NMOS switches may be controlled by different control signals, e.g. by digital code words \( P_{1} \) to \( P_{n} \) and \( N_{1} \) to \( N_{n} \), respectively. This allows a different number of PMOS and NMOS transistors from the complementary sets to be connected to supply rails, thereby changing the ratio of PMOS and NMOS transistors comprised in buffer circuit 21. Changing this ratio shifts the VTC of the resulting buffering circuit along the X-axis. This way, the VTC of the DC-coupled oscillator buffer 21 can be shifted by digitally controlling the transistors ratio \( W_{P}/W_{N} \) of the inverter to cover VTC variations. More in detail, switching more PMOS transistors moves the VTC and hence its point of maximum sensitivity to the right along the X-axis, while switching more NMOS transistors causes the VTC and hence the maximum sensitivity point to shift to the left. As a change in the ratio between switched PMOS and NMOS transistors results in shifting the VTC along the X-axis, switching a number of equally sized PMOS and NMOS transistors does not affect (move) the VTC of the buffering circuit, as the overall transistor ratio \( W_{P}/W_{N} \) which determines the position of VTC, remains unchanged. Increasing this ratio moves the VTC towards VDD (right) and decreasing moves it towards GND (left). Fig. 6 shows an example implementation of the oscillator buffer, where the transistors forming the complementary set have the same sizes, i.e. each NMOS transistor has a gate width of \( W_{n} \) and each PMOS transistor a gate width of \( W_{p} \). Another possible implementation of the oscillator buffer is shown in Fig. 7 where the PMOS/NMOS transistors are binary weighted.

The number of transistors and their gate width should be sized accordingly to account for PVT variations and the load to be driven. The variation in DC level of the oscillator output is estimated via circuit simulations across process corners representing the extremes of the parameter variations (such as doping concentrations, length, width etc.). The extremes represent the case when all the process variations either deviate towards a transistor with reduced currents (slow corner) or increased currents (fast corner). The number and width of the switchable PMOS and NMOS transistors is then chosen to cover this variation with an extra margin (e.g. 5%). For example, in Fig. 6, when the n-bit control word for both the PMOS and NMOS switches is (0000 ... 1), all the switches except for \( P_{n} \) and \( N_{1} \) are off. Hence, only the transistors connected to these switches comprise the buffer leading to an overall transistor ratio \( W_{P}/W_{N} \). When the code words for PMOS and NMOS switches are (1100 ... 1) and (1000 ... 0), then the switches \( P_{1} \), \( P_{2} \), \( P_{n} \) and \( N_{1} \) are on. Hence, the transistor ratio in this case is increased to \( 3W_{P}/W_{N} \). Similarly, if the code words for PMOS and NMOS switches are (1000 ... 1) and (1100 ... 1), the transistor ratio is decreased to \( 2W_{P}/3W_{N} \).

Fig. 8 shows the schematic of an embodiment of the proposed buffer with digitally tuneable VTC. The buffer com-
primes a default complementary pair of PMOS and NMOS transistor and four PMOS and NMOS transistors with binary weighted widths serving as the tuneable inverters. In this implementation, the default pair is always connected to supply rails and thus provides an initial value of buffer’s $W_n/W_p$ ratio. The binary weighted transistors are controlled by a single 5-bit digital word. When the input code is “00000”, none of the additional transistors are connected, but the default complementary pair. This default pair is sized at five times that of the smallest switchable pair to drive the subsequent load while operating at the maximum sensitivity point for an input DC level corresponding to the typical corner. The MSB of the 5-bit buffer control determines whether PMOS or NMOS need to be turned on, while the 4 LSB bits determine how many of those transistors are turned on. For example, for a single control word (11010), the MSB ‘1’ indicates that PMOS transistors should be on and the 4-LSB ‘1010’ indicate that switches P2 and P4 are on. Similarly, for a single control word (01010), the MSB ‘0’ indicates that NMOS transistors should be on and the 4-LSB ‘1010’ indicate that switches N2 and N4 are on. This is just one possible implementation of the way the ratio $W_n/W_p$ is controlled and the skilled person will readily find alternative implementations. It is possible for example to have separate 4-bit control words for PMOS and NMOS transistors rendering more flexibility as illustrated in FIG. 6 and FIG. 7. By monitoring the duty cycle of the buffer output signal the control code (5-bit binary for e.g. 10100) that shifts the VTC to the desired position is generated. At the optimal biasing point, the duty cycle of the oscillator output is 50%. The precision with which the VTC can be shifted, is determined by the smallest possible change in the ratio $W_n/W_p$. If the input DC level is larger than the optimum point (corresponding to $V_{out}$), the digital control enables more PMOS transistors such that the buffer’s VTC shifts to the right. Similarly, if the input DC level is smaller than the optimal point, more NMOS transistors are enabled to shift the VTC towards the left.

The subsequent buffer 22 in FIG. 4 is used because a large load needs to be driven. In its absence, the default pair of the tuneable buffer should be very large. This in turn warrants large sizes for additional transistors to alter the $W_n/W_p$ significantly, leading to a larger overall buffer size. To summarize, the first buffer brings the low-input swing to a large load needs to be driven. In its absence, the default pair of the tuneable buffer should be very large. This in turn warrants large sizes for additional transistors to alter the $W_n/W_p$ significantly, leading to a larger overall buffer size. To summarize, the first buffer brings the low-input swing to a low-input swing. Thus, this buffer can operate with any input DC-voltage between 325 mV to 425 mV. Hence, the proposed DC-coupled buffer can operate with low input-swing notwithstanding the process variations.

While the present disclosure has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive. The foregoing description details certain embodiments of the disclosure. It will be appreciated, however, that no matter how detailed the foregoing appears in text, the disclosure may be practiced in many ways. The disclosure is not limited to the disclosed embodiments.

Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed disclosure, from a study of the drawings, the disclosure and the appended claims. In the claims, the word “comprising” does not exclude other elements or steps, and the indefinite article “a” or “an” does not exclude a plurality. A single processor or other unit may fulfill the functions of several items recited in the claims. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage. A computer program may be stored/distributed on a suitable medium, such as an optical storage medium or a solid-state medium supplied together with or as part of other hardware, but may also be distributed in other forms, such as via the Internet or other wired or wireless telecommunication systems. Any reference signs in the claims should not be construed as limiting the scope.

1. A buffering circuit for buffering an oscillator signal, the buffering circuit comprising:

- a plurality of PMOS and NMOS transistor pairs connected in parallel, each pair having connected gate terminals and connected drain terminals forming an inverter circuit, each pair arranged for receiving via a direct coupling a sinusoidal oscillator signal with a variable DC level at its gate terminal, and each pair further being connected with an additional PMOS and NMOS transistor; and

- a control circuit arranged for receiving an output signal output by the inverter circuit, for deriving information on the DC level of the output signal, and for adjusting a voltage transfer curve expressing a relationship between a voltage at the input and output of the buffering circuit.
to match the variable DC level, by switching on or off the additional PMOS and NMOS transistors based on the derived information.

2. The buffering circuit as in claim 1, wherein the control circuit is arranged for deriving the information on the DC level by averaging the output signal.

3. The buffering circuit as in claim 1, wherein the inverter circuit is implemented in CMOS.

4. The buffering circuit as in claim 1, wherein gate widths of transistors belonging to different pairs have a ratio being a power of 2, so that the transistor pairs of the plurality are sized to form binary weights.

5. The buffering circuit as in claim 1, wherein the control circuit is arranged for adjusting the DC level by generating code words.

6. A device comprising an oscillator and a buffering circuit as in claim 1.

7. The device as in claim 6, wherein the oscillator is a voltage controlled oscillator or a digitally controlled oscillator.

8. The device as in claim 6, comprising a further buffer arranged for receiving the output signal of the buffering circuit.

9. The device as in claim 6, wherein the oscillator is part of a phase-locked loop.

10. A method for calibrating a buffering circuit comprising:
    applying via a direct coupling a sinusoidal oscillator signal with variable DC level to a circuit comprising a plurality of PMOS and NMOS transistor pairs connected in parallel, each pair having connected gate terminals and connected drain terminals forming an inverter circuit, each pair arranged for receiving the oscillator signal at its gate terminal, and each pair further being connected with an additional PMOS and NMOS transistor,
    deriving information on the DC level of an output signal output by the inverter circuits; and
    adjusting a voltage transfer curve expressing a relationship between a voltage at the input and output of the buffering circuit to match the variable DC level, by switching on or off the additional PMOS and NMOS transistors based on the derived information.

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