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(54) **METHOD AND APPARATUS FOR ASYNCHRONOUS CLOCK RETIMING**

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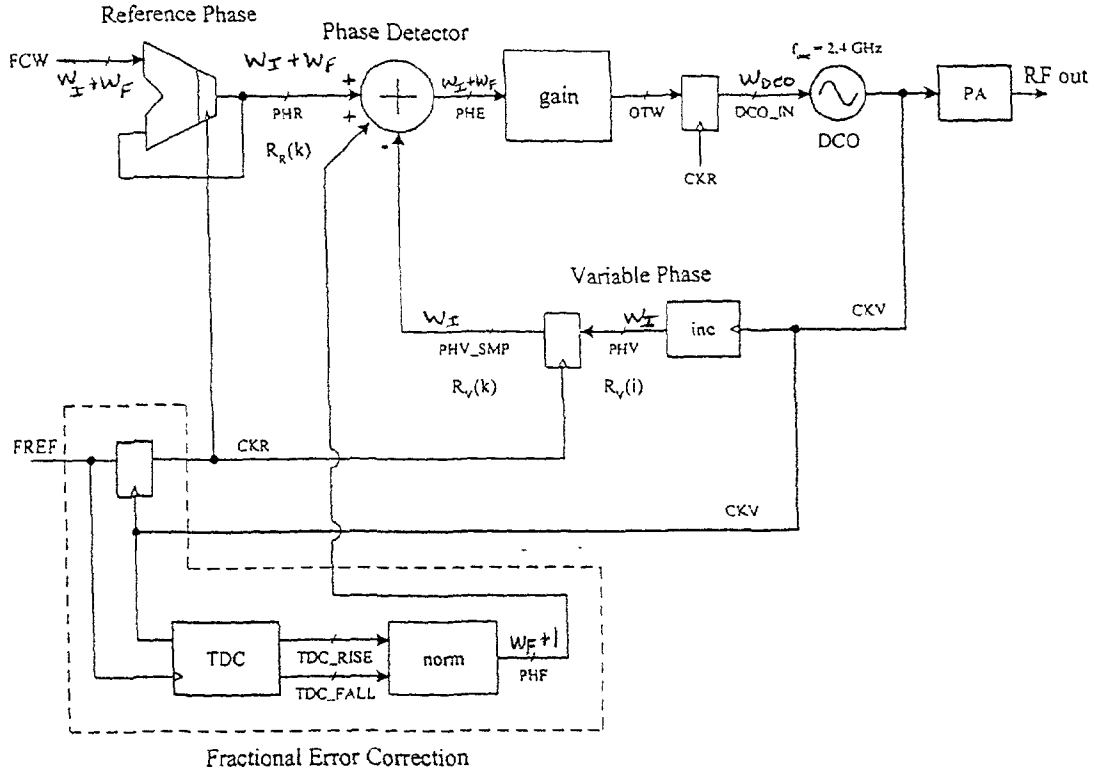
(52) **U.S. Cl.** **375/355**

(57) **ABSTRACT**

A time to digital converter is used to determine which edge of the higher frequency clock (oversampling clock) is farther away from the edge of the lower frequency timing signal. At the same time, the oversampling clock performs sampling of the timing signal by two registers: one on the rising edge and the other on the falling edge. Then, the register of "better quality" retiming, as determined by the fractional phase detector decision, is selected to provide the retimed output.



Fractional Error Correction

FIG. 1

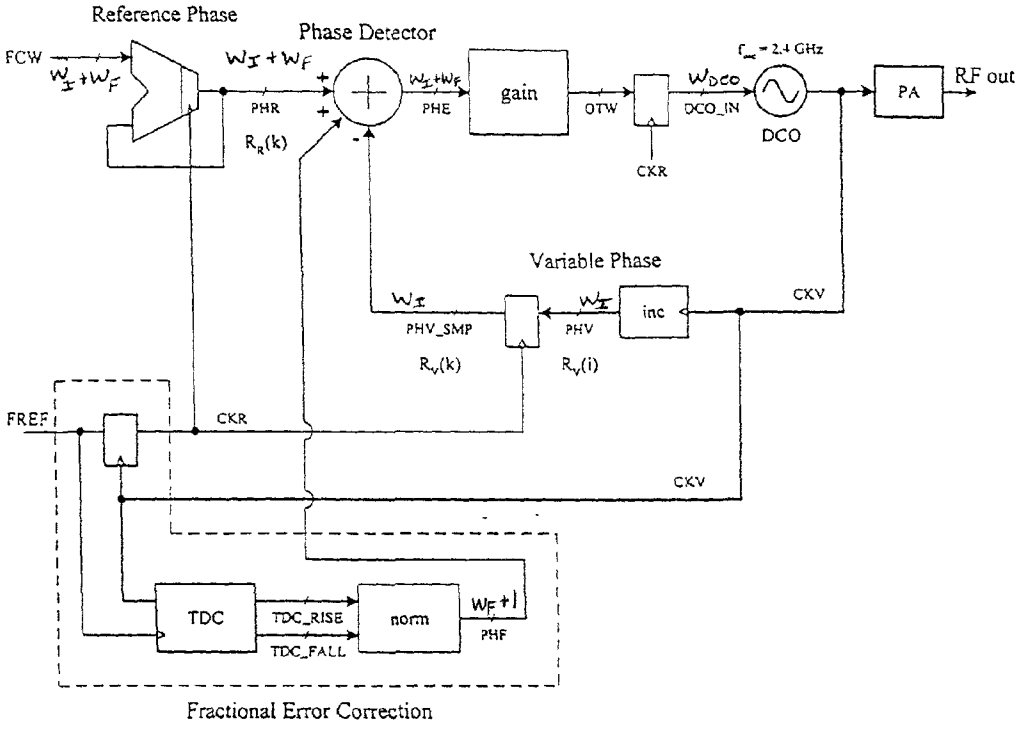

Reference Phase
Phase Detector
FCW
W_I+W_F
PHR
$R_R(k)$
PHE
gain
OTW
CKR
W_{DCO}
DCO_IN
DCO
f_{out} = 2.4 GHz
PA
RF out
Variable Phase
PHV_SMP
$R_v(k)$
PHV
$R_v(i)$
inc
CKV
FREF
TDC
TDC_RISE
TDC_FALL
norm
W_F+1
PHF
Fractional Error Correction

FIG. 2

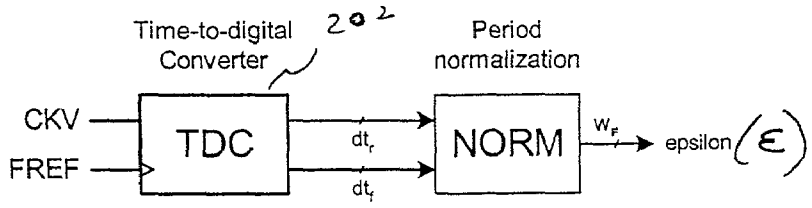


FIG. 3

Negative fractional phase error:

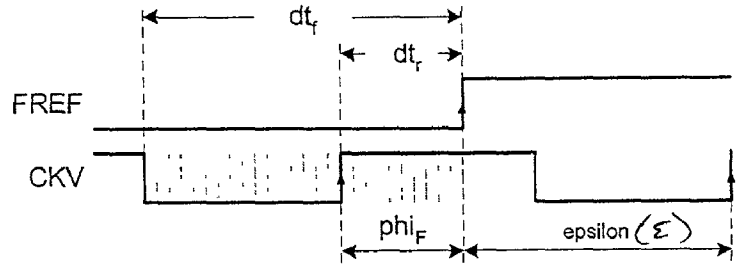


FIG. 4

Positive fractional phase error:

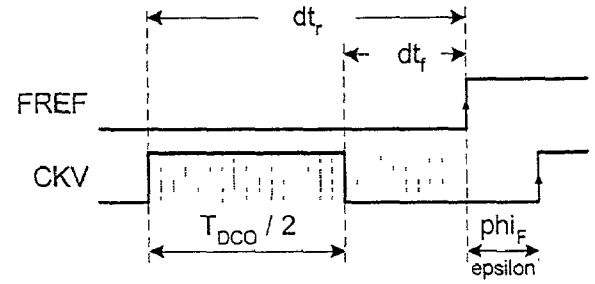


FIG. 5

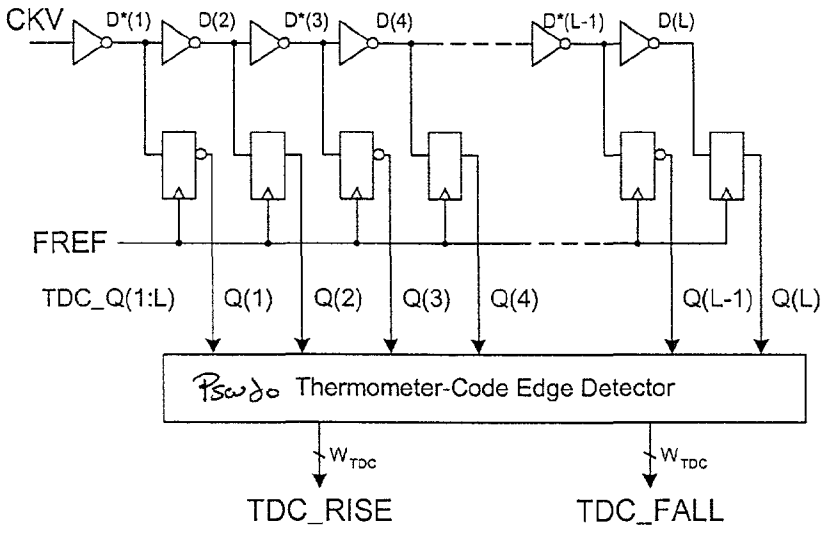

CKV
D*(1)
D(2)
D*(3)
D(4)
D*(L-1)
D(L)
FREF
TDC_Q(1:L)
Q(1)
Q(2)
Q(3)
Q(4)
Q(L-1)
Q(L)
Thermometer-Code Edge Detector
W_TDC
W_TDC
TDC_RISE
TDC_FALL

FIG. 6

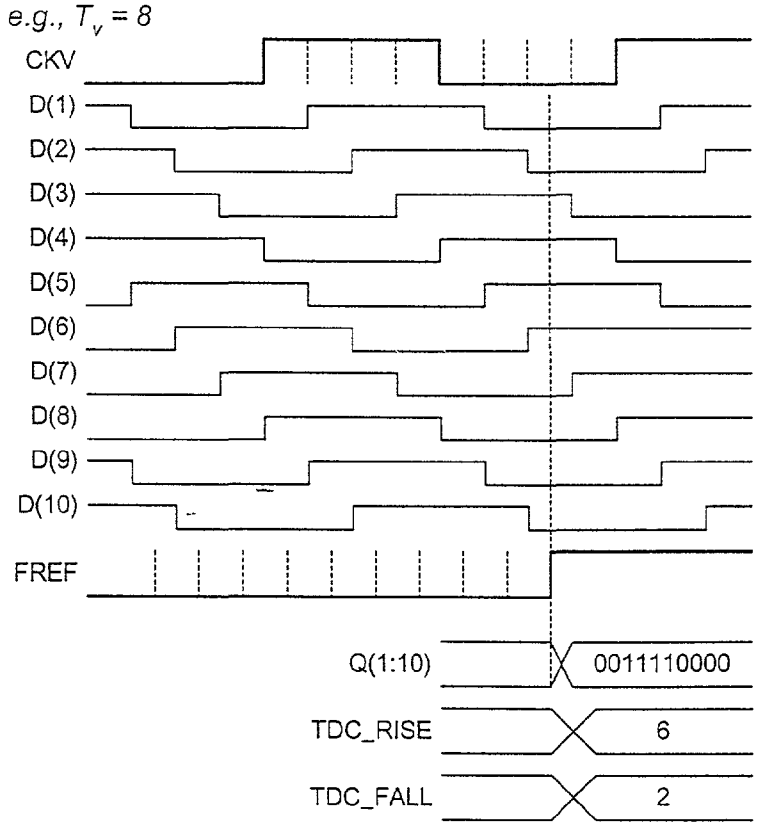

e.g., T_v = 8
CKV
D(1)
D(2)
D(3)
D(4)
D(5)
D(6)
D(7)
D(8)
D(9)
D(10)
FREF
Q(1:10)
0011110000
TDC_RISE
6
TDC_FALL
2

FIG. 7

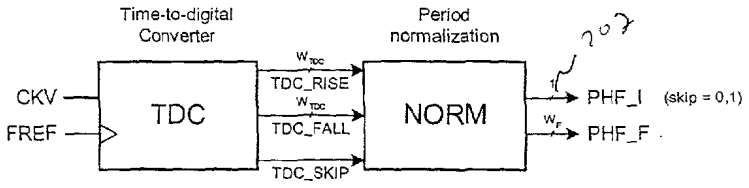

Time-to-digital Converter
Period normalization
207
CKV
FREF
TDC
w_{TDC}
TDC_RISE
w_{TDC}
TDC_FALL
TDC_SKIP
NORM
PHF_I (skip = 0,1)
w_F
PHF_F

FIG. 8

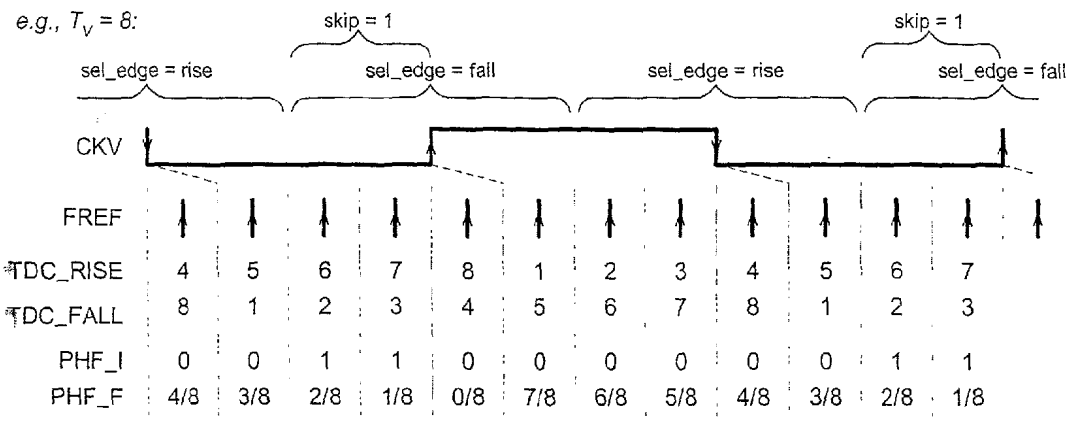

e.g., T_V = 8:
skip = 1
skip = 1
sel_edge = rise
sel_edge = fall
sel_edge = rise
sel_edge = fall
CKV
FREF
TDC_RISE 4 5 6 7 8 1 2 3 4 5 6 7
TDC_FALL 8 1 2 3 4 5 6 7 8 1 2 3
PHF_I 0 0 1 1 0 0 0 0 0 0 1 1
PHF_F 4/8 3/8 2/8 1/8 0/8 7/8 6/8 5/8 4/8 3/8 2/8 1/8

FIG. 9

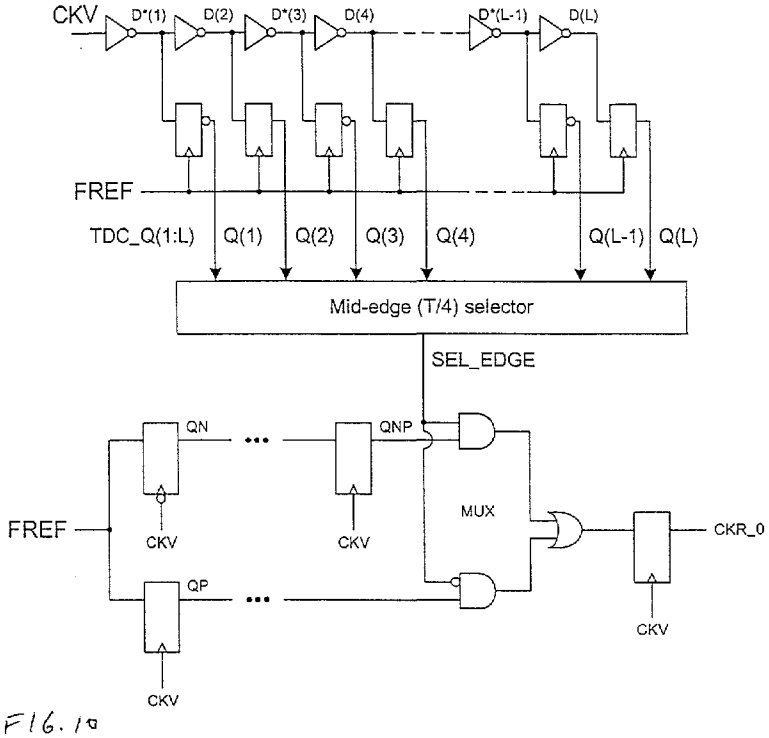

CKV
D*(1)
D(2)
D*(3)
D(4)
D*(L-1)
D(L)
FREF
TDC_Q(1:L)
Q(1)
Q(2)
Q(3)
Q(4)
Q(L-1)
Q(L)
Mid-edge (T/4) selector
SEL_EDGE
QN
QNP
FREF
CKV
CKV
MUX
CKR_0
QP
CKV
CKV

FIG. 10

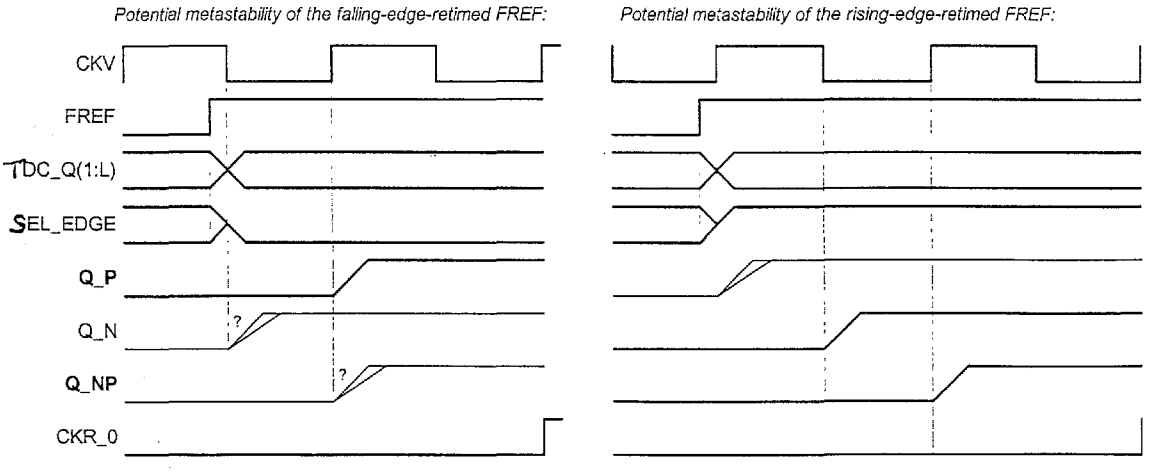

Potential metastability of the falling-edge-retimed FREF:
Potential metastability of the rising-edge-retimed FREF:
CKV
FREF
TDC_Q(1:L)
SEL_EDGE
Q_P
Q_N
Q_NP
CKR_0
?
?

FIG. 11

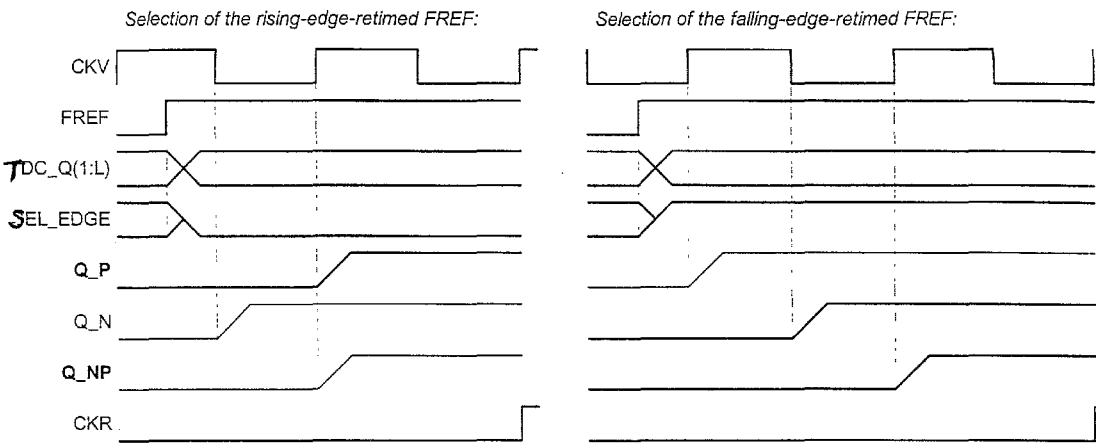


FIG. 12

e.g., N=16

TDC_Q(11)	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1
TDC_Q(10)	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
TDC_Q(9)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
TDC_Q(8)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
TDC_Q(7)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0
TDC_Q(6)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0
TDC_Q(5)	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
TDC_Q(4)	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
TDC_Q(3)	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
TDC_Q(2)	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
TDC_Q(1)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
CKV																									
PHF_I	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	
PHF_F	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

0 = rising
1 = falling
SEL_EDGE

METHOD AND APPARATUS FOR ASYNCHRONOUS CLOCK RETIMING

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/242,577, entitled "Asynchronous Clock Retiming Method", having attorney docket No. TI-32077PS, and filed on Oct. 23,2000.

TECHNICAL FIELD

[0002] This invention relates in general to the field of electronics and more specifically to a method for asynchronous clock retiming.

BACKGROUND

[0003] Retiming a lower frequency timing signal (or clock) by a higher frequency clock, when both signals are asynchronous to each other, is typically done by passing the lower frequency signal through a series of registers (e.g., flip-flops) that are clocked using the higher frequency clock. There is however, a certain probability of a metastability condition per register stage and the overall probability of metastability at the system output increases exponentially with each register stage used. The number of registers is established such that the Mean Time Between Failures (MTBF) rate is acceptably small.

[0004] Unfortunately, the metastability condition brings the timing uncertainty of one high speed clock (or possibly higher) since, during metastability, the output could be resolved at a given clock or at the next. Although the output levels are defined, this timing error is unacceptable in some applications. A need thus exist in the art for a method for asynchronous clock retiming that can overcome some of the problems mentioned above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The features of the present invention, which are believed to be novel, are set forth with particularity in the appended claims. The invention, may best be understood by reference to the following description, taken in conjunction with the accompanying drawings, in the several figures of which like reference numerals identify like elements, and in which:

[0006] **FIG. 1** shows a block diagram of a phase-domain all-digital synchronous PLL synthesizer that uses the present invention.

[0007] **FIG. 2** shows a time-to-digital converter (TDC) and period normalization block, forming a fractional phase detector.

[0008] **FIG. 3** shows a timing diagram highlighting a negative fractional phase error condition.

[0009] **FIG. 4** shows a timing diagram highlighting a positive fractional phase error condition.

[0010] **FIG. 5** shows a circuit that is used to determine the "raw" digital fractional phase.

[0011] **FIG. 6** shows a timing diagram for the circuit shown in **FIG. 5**.

[0012] **FIG. 7** shows a TDC and period normalization block that provide for edge skipping.

[0013] **FIG. 8** shows a timing diagram for the circuit shown in **FIG. 7**.

[0014] **FIG. 9** shows a DCO clock retiming circuit in accordance with the invention.

[0015] **FIG. 10** shows a timing diagram for the circuit in **FIG. 9**.

[0016] **FIG. 11** shows the selection of the rising-edge-retimed FREF signal or the falling-edge-retimed FREF in accordance with the invention.

[0017] **FIG. 12** shows details of the DCO clock retiming in accordance with the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0018] While the specification concludes with claims defining the features of the invention that are regarded as novel, it is believed that the invention will be better understood from a consideration of the following description in conjunction with the drawing figures.

[0019] The method described herein is a general solution to the problem of retiming a lower frequency timing signal (or clock) by a higher frequency clock when both signals are asynchronous to each other. In the following described embodiment, the timing signal is a Frequency-Reference clock (FREF), the oversampling clock is a Digitally-Controlled Oscillator (DCO) clock output. Obviously, both of these signals are completely asynchronous to each other. The preferred embodiment will describe the invention in association with a frequency synthesizer based on a phase-domain All-Digital-Phase-Lock-Loop (ADPLL) structure although the invention can be used in any application where an asynchronous clock retiming is required. A block diagram of an ADPLL synthesizer **100** that can use the present invention is shown in **FIG. 1**. The PLL loop is a fixed-point phase-domain architecture whose purpose is to generate an RF frequency in the 2.4 GHz Bluetooth band. The central element in synthesizer **100** is a digitally-controlled oscillator (DCO) and the PLL loop used is a fully digital and of type I (i.e., only one integrating pole due to the DCO frequency-to-phase conversion). The PLL loop arithmetically compares the accumulated frequency control word (FCW) in the reference phase accumulator $R_R(k)$ in order to arrive at the phase error correction. The FCW input to the reference accumulator is used to establish the operating frequency of the desired channel, and it is expressed in a fixed-point format such that 1 LSB of its integer part corresponds to the f_R reference frequency.

[0020] A more detailed discussion of the synthesizer section can be found in a U.S. patent application entitled "Digital Phase-Domain PLL Frequency Synthesizer", by Staszewski, et al., having Ser. No. 09/603,023, filed on Jun. 26, 2000, this application is incorporated by reference as if fully set forth herein. A more detailed discussion of the fractional phase detector used in synthesizer **100** can be found in a U.S. patent application entitled "Digital Fractional Phase Detector", by Staszewski, et al., having Ser. No. 09/608,317, filed on Jun. 30, 2000, this application is incorporated by reference as if fully set forth herein.

[0021] In the ADPLL **100** the reference phase, variable (DCO) phase, phase error, and all other phase signals need to be represented as fixed-point digital word signals that are synchronous to each other and cannot be corrupted by noise. If this is accomplished, then the phase error can be simply an output of a synchronous arithmetic subtractor used as a phase detector. Thus retimed FREF clock (CKR) is used as a synchronous clock.

[0022] The ADPLL **100** uses a selection control circuit such as a time-to-digital converter (TDC) **202** to measure the fractional (sub-T_v) delay difference between both edges of the DCO clock and the reference clock with a time quantization and resolution of Δt_{res}. This difference is represented by a digital word, the timing diagram for a negative phase error are shown in **FIG. 3**, while the timing diagram for a positive phase error are shown in **FIG. 4**.

[0023] The digital fractional phase is determined by passing the DCO clock through a chain of inverters as shown in **FIG. 5**, such that each inverter output produces a clock signal slightly delayed than from the previous inverter. The staggered clock phases are then sampled by the same reference clock. Position of the detected transition from a logic 1 to a logic 0 indicates that a quantized time delay Δt_r between the FREF sampling edge and the rising edge of the DCO clock, CKV, in Δt_{res} multiples. Similarly, position of the detected transistion from a logic 0 to a 1 indicates a quantized time delay Δt_f between the FREF sampling edge and the falling edge of the DCO clock, CKV. Because of the time-casual nature of this operation, both delay values must be interpreted as positive. This is fine if Δt_r is samller than Δt_f. This corresponds to the negative phase error of the classical PLL loop in which the DCO edge is ahead of the reference edge and, therefore, the phase sign has to be negated. However, it is not so straightforward if Δt_r is greater than Δt_f, which correponds to the positive phase error of the classical PLL loop.

[0024] The time lag between the reference edge and the following rising edge of the CKV must be calculated based on the available information of the delay between the preceeding rising edge of CKV and the reference edge and the clock half-period, which is the difference $T_v/2 = \Delta t_r - \Delta t_f$. In general,

$$T_v/2 = \Delta t_r - \Delta t_f \text{ if } \Delta t_r \geq \Delta t_f, \text{ otherwise } \Delta t_f - \Delta t_r.$$

[0025] The above analysis can be summarized in equation in the following equation, where Δt_{frac} is the digital fractional phase detector output:

$$\Delta t_{frac} = -\Delta t_r \text{ if } \Delta t_r \geq \Delta t_f, \text{ otherwise } \Delta t_r - 2\Delta t_f.$$

[0026] The period-normalized fractional phase is described by:

$$\phi F = \frac{\Delta t_{frac}}{T_v}.$$

[0027] In this implementation, the fractional phase is not needed. Instead, Δt_r is used as the $\epsilon(k)$ correction that is positive and $\epsilon \in (0, 1)$, in the following equation: $\theta_r(k) = k \cdot N + \theta_0 + \epsilon(k)$, where $\theta_r(k)$ is the reference phase, k is an index, the $\theta_v(k)$ is the high-rate DCO phase, and $\epsilon(k) = \Delta t_r(k) T_v$.

[0028] In practice, it is preferred to obtain the clock period through longer-term averaging in order to ease the calculation burden and linearize the transfer function of $1/T_v$. The averaging time constant can be as slow as the expected drift of the inverter delay.

[0029] The actual fractional output of the error correction "ϵ" needs one extra bit due to the fact that the whole CKV cycle has to be skipped, if the rising edge of FREF transitions is too close before the rising edge of CKV and, as a safety precaution, the falling CKV edge has to be used. This scenario is illustrated in **FIGS. 7 and 8**. Output PHF_I **702** is of the integer least-significant-bit (LSB) weight.

[0030] The clock retiming solution in accordance with the invention uses the previously-described TDC circuit to determine which edge of the higher frequency clock (oversampling clock) is -farther away, or far enough based on the design criteria, from the edge of the lower frequency timing signal. Alternatively, in another design, the circuit only needs to find an edge that is far enough to guarantee a low probability of metastability. In this case, it could well be that either edge meets a "far enough" threshold. This predetermined threshold can be determined on a design by design case, and it is usually acceptable for timing values larger than several inverter delays. At the same time, the oversampling clock performs sampling of the timing signal by two registers, one on the rising edge and the other on the falling edge. Then the register of "better quality" retiming, as determined by the fractional phase detector decision, is selected to provide the retimed output.

[0031] In **FIG. 9**, there is shown a circuit that allows for the ADPLL **100** to synchronize the reference and variable clock signals in accordance with the invention. Both of the retimed signal paths are provided to a selection circuit such as a multiplexer (mux). In **FIG. 10**, there is shown the potential metastability of the falling-edge-retimed FREF and the potential metastability of the rising-edge-retimed FREF. The sole purpose is to resample the reference clock with a variable DCO clock as required in order to avoid metastability. It does so by resampling the FREF by both edges of CKV and choosing the one that has the larger clock separation. The select decision is based on the existing TDC output, thus little additional cost is incurred. In case of FREF resampling with the falling edge of CKV, an additional rising-edge CKV retiming is required.

[0032] A high degree of redundancy in the thermometer-encoded TDC output vector could be exploited to obtain extra error correction and metastability resolution. However, in the preferred embodiment we have chosen a simple extraction of the selection control. In **FIG. 11** there is shown a timing diagram highlighting the selection of the rising-edge-retimed FREF signal and the selection of the falling-edge-retimed FREF signal. **FIG. 12** highlights how a certain single TDC register output can be used for the edge selection. It is also shown in FIGS. **7-12** that it is necessary to skip the whole CKV clock cycle if the FREF rising edge is close to the CKV rising edge. Consequently, an extra bit of information is sent to the phase detector. Several additional pairs of rising/falling reclocking stages are inserted to allow extra time (in multiple of CKV clock cycles) for the SEL_EDGE selection signal to resolve its metastability.

[0033] The asynchronous retiming method of the present invention begins by sampling the frequency reference clock (FREF) using both edges of an oversampling clock (CKV) that is derived from a controllable oscillator, such as a DCO.

The sampling is preferably performed by a pair of clocked memory elements, such as flip-flops or registers, one operating on the positive or rising transition of the CKV clock, and the other operating on the negative or falling transition of the CKV clock. The effect of sampling the FREF clock by the CKV clock is to retime the FREF to either the rising or falling edge of the CKV clock.

[0034] By using a circuit like a time-to-digital converter to determine which edge of a higher frequency clock (e.g., oversampling clock) is farther away from the significant edge of the lower frequency timing signal, provides for improved asynchronous clock retiming. When the retiming method of the present invention is used in an all-digital PLL synthesizer, as one example, the retimed FREF can be used as a synchronous clock for the synthesizer. The retimed frequency reference (CKR) can be generated using a digitally-controlled oscillator (DCO) output as the oversampling clock. Thus providing for an improved and lower cost design.

What is claimed is:

1. A method for asynchronous retiming using a lower frequency clock signal (FREF), and an oversampling clock signal (CKV), comprising the steps of:

sampling the FREF using both the rising and falling edges of the CKV to produce first and second retimed FREF signals; and

selecting from either the first or second retimed FREF signals one that provides a predetermined level of low metastability.

2. A method as defined in claim 1, wherein the sampling step comprises sampling by the rising edges of the CKV using a first clocked memory element and sampling by the falling edges of the CKV using a second clocked memory element.

3. A method as defined in claim 2, wherein the first and second clocked memory elements comprise registers or flip-flops.

4. A method as defined in claim 2, wherein the retiming step produces both rising and falling edge retimed signal paths, and the method further comprising the step of:

providing both the rising and falling edge retimed signal paths to a selection circuit.

5. A method as defined in claim 4, further comprising the step of:

delaying both the rising and falling edge retimed signal paths by a controllable amount.

6. A method as defined in claim 5, wherein the delaying step is performed by introducing a predetermined number of shift register stages that are clocked by the CKV or a clock signal derived from the CKV.

7. The method as defined in claim 4, wherein the selection circuit comprises a multiplexer.

8. The method as defined in claim 7 wherein the multiplexer has an output that is resampled by the CKV.

9. The method as defined in claim 2, wherein the retiming step produces both rising and falling edge retimed signal paths, and further comprising the step of:

choosing from either the rising or falling edge signal paths, the signal path that is furthest away from metastability.

10. The method of claim 9, wherein the choosing step is performed by a mid-edge detector that comprises a time-to-digital converter (TDC) that is clocked by the FREF.

11. The method of claim 9, wherein the choosing step is performed by a mid-edge detector that determines which one of the two CKV edges lies farther away from an edge of the FREF.

12. The method of claim 1, further comprising the steps of:

delaying the CKV;

sampling the delayed CKV using the FREF such that the selected retimed signal is sufficiently away from a metastability condition.

13. The method of claim 1, wherein the oversampling clock signal (CKV) is an oscillator output and the lower frequency clock signal (FREF) is a frequency reference signal.

14. A circuit for asynchronous retiming using a first clock signal and a second clock signal, said second clock signal having a higher frequency than the first clock signal, the circuit comprising:

a sampling circuit for sampling the first clock signal using both edges of the second clock signal and producing first and second retimed signals; and

a selection control circuit coupled to the sampling circuit for selecting from the first and second retimed signals the signal that provides at least a predetermined level of low metastability.

15. A circuit as defined in claim 14, wherein the sampling circuit comprises a pair of clocked memory elements.

16. A circuit as defined in claim 14, wherein the selection control circuit comprises a time-to-digital converter (TDC).

17. A circuit as defined in claim 16, wherein the TDC selects which of the first and second retimed signals to select by determining which edge of the second clock signal is farther away from a significant edge of the first clock signal.

18. A circuit as defined in claim 14, further comprising:

a delay circuit coupled to the selection circuit for delaying the first and second retimed signals.

19. A circuit as defined in claim 18, wherein the delay circuit comprises at least one shift register.

20. A circuit as defined in claim 14, further comprising a multiplexer coupled to the selection control circuit.

* * * * *