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Entezari et al.

(54) **MINIMIZATION OF RMS PHASE ERROR IN A PHASE LOCKED LOOP BY DITHERING OF A FREQUENCY REFERENCE**

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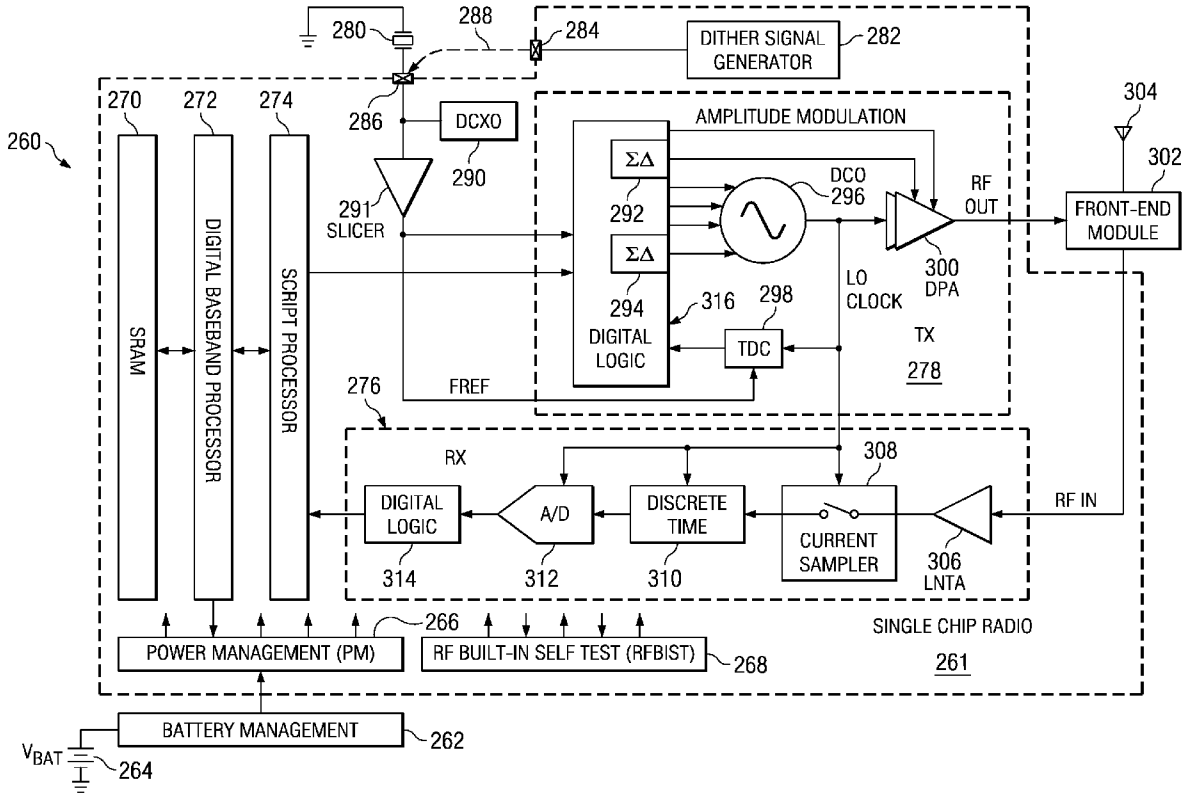
H04B 1/04 (2006.01)

(52) **U.S. Cl.** **455/114.2**

(57) **ABSTRACT**

A novel and useful apparatus for and method of minimizing the phase distortions experienced at the output of a phase locked loop (PLL) by dithering of its input frequency reference to overcome additive interference that is parasitically suffered on it. The frequency reference signal is dithered in a controlled manner using either indirect or direct coupling. The dither signal may be a single clock or is generated by switching between two or more of the existing clock signals generated, or may be produced by a dedicated pseudo-random noise generator having specific spectral properties. In indirect coupling, the dither signal is coupled through a bond wire sufficiently close in proximity to the frequency reference circuit input. This dominates the jitter inflicted onto the frequency reference signal and upconverts its spectral content to higher frequency, thus eliminating the more damaging low-frequency jitter caused by the interfering RF signal. In direct coupling, the dither signal is coupled to the reference frequency input using a network of components directly connected thereto.



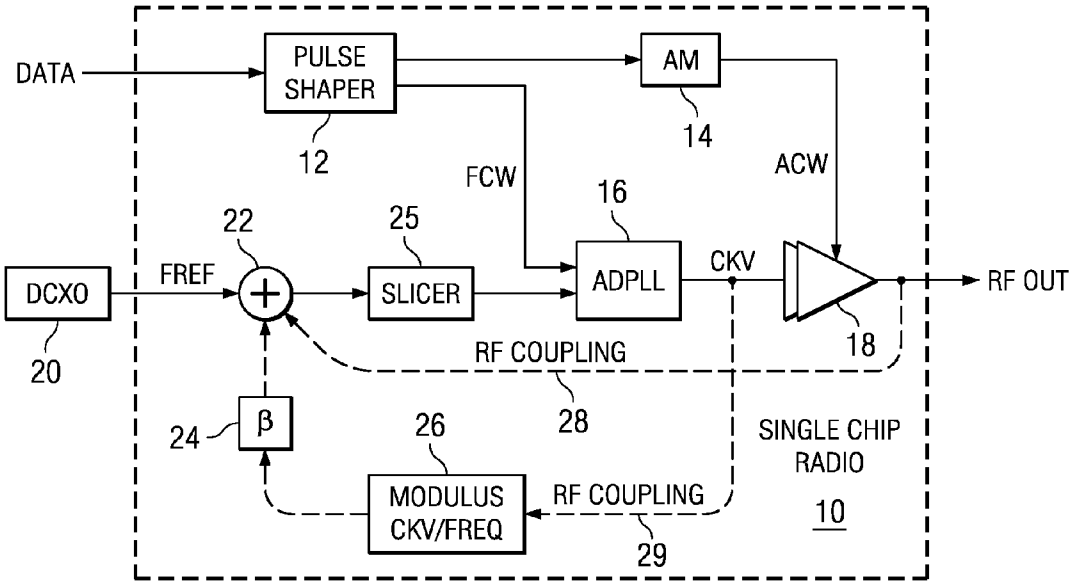


FIG. 1
(PRIOR ART)

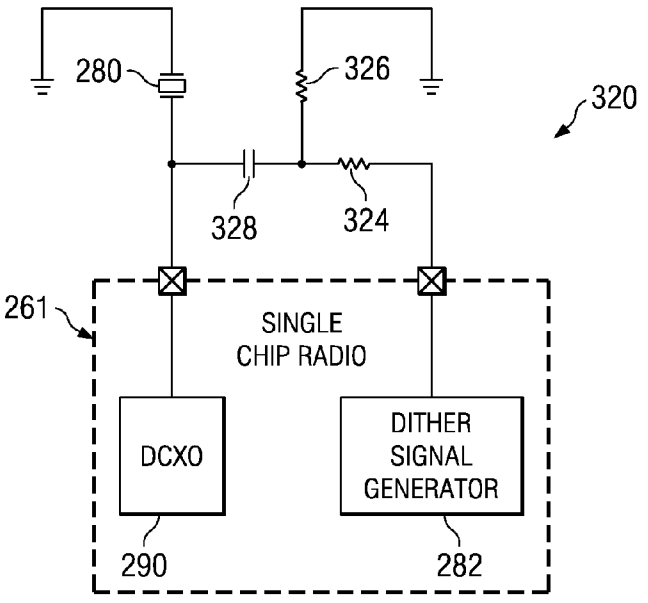


FIG. 2B

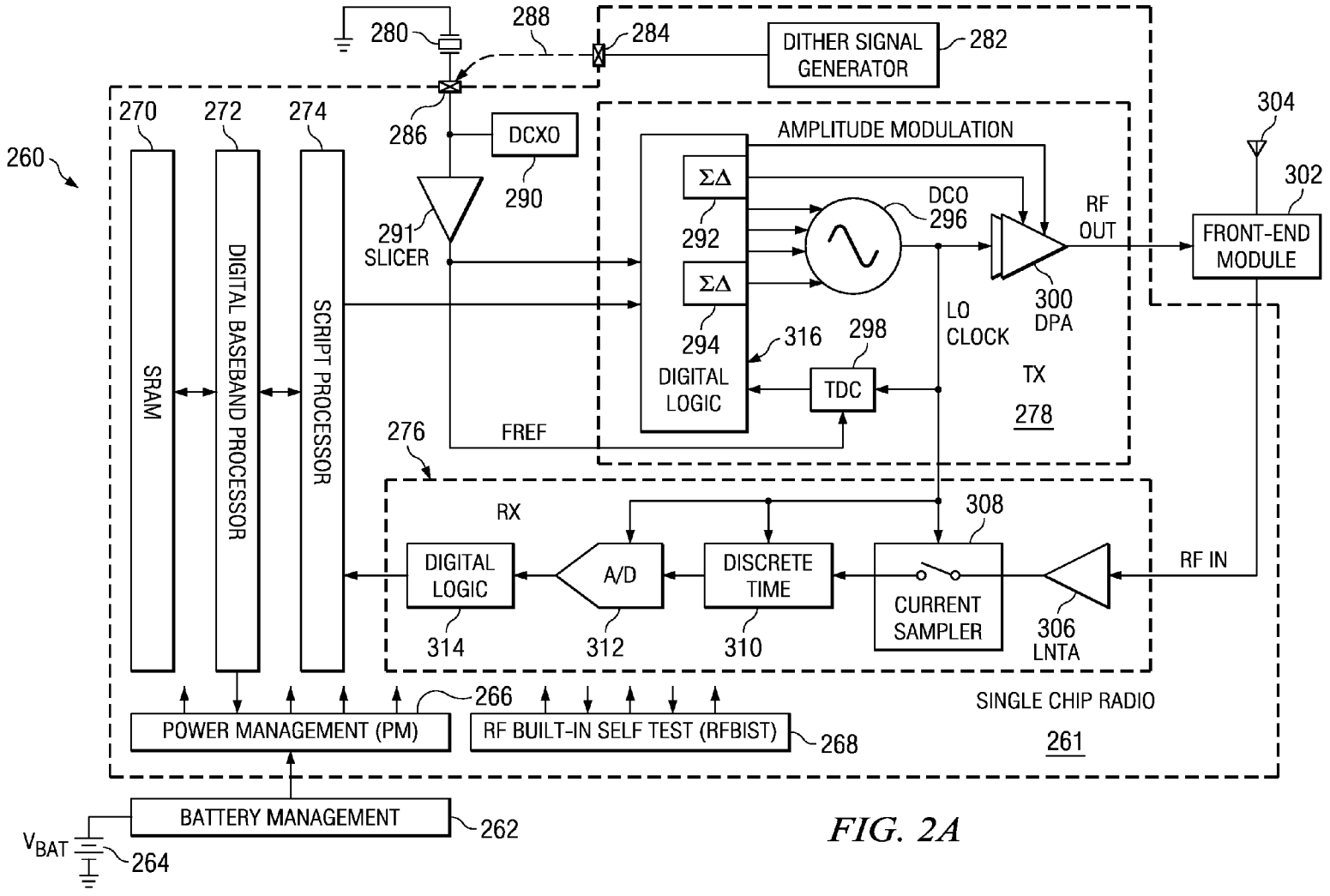

260
270
272
274
SRAM
DIGITAL BASEBAND PROCESSOR
SCRIPT PROCESSOR
280
288
284
DITHER SIGNAL GENERATOR
282
286
DCXO
290
291
SLICER
AMPLITUDE MODULATION
ΣΔ
292
ΣΔ
294
DIGITAL LOGIC
DCO
296
RF OUT
300
DPA
LO CLOCK
316
298
TDC
TX
278
276
FREF
304
302
FRONT-END MODULE
RX
308
DIGITAL LOGIC
314
A/D
312
DISCRETE TIME
310
CURRENT SAMPLER
306
LNTA
RF IN
266
POWER MANAGEMENT (PM)
RF BUILT-IN SELF TEST (RFBIST)
268
SINGLE CHIP RADIO
261
BATTERY MANAGEMENT
262
VBAT
264

FIG. 2A

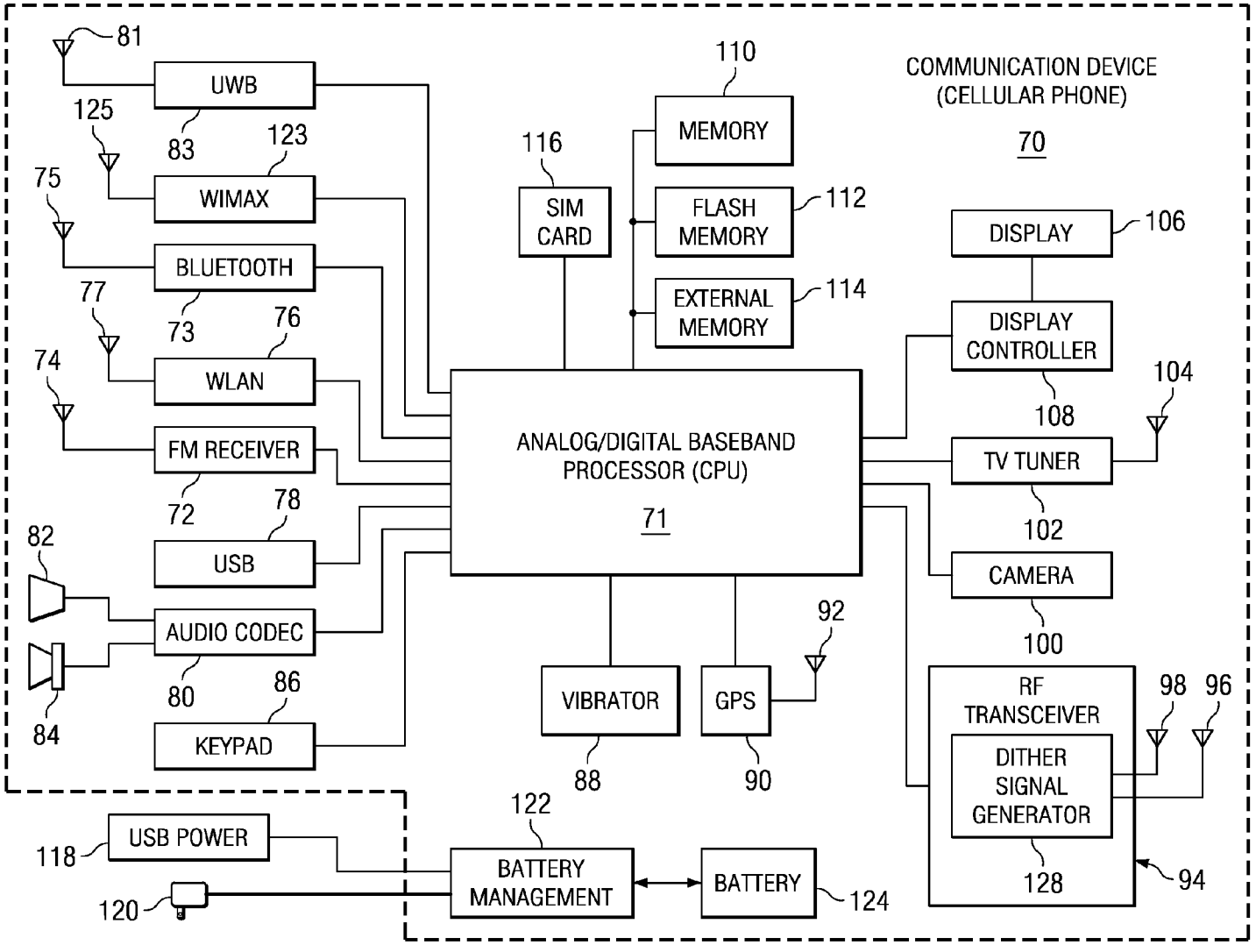

COMMUNICATION DEVICE
(CELLULAR PHONE)
70
ANALOG/DIGITAL BASEBAND
PROCESSOR (CPU)
71
UWB
WIMAX
BLUETOOTH
WLAN
FM RECEIVER
USB
AUDIO CODEC
KEYPAD
MEMORY
SIM CARD
FLASH MEMORY
EXTERNAL MEMORY
DISPLAY
DISPLAY CONTROLLER
TV TUNER
CAMERA
RF TRANSCEIVER
DITHER SIGNAL GENERATOR
VIBRATOR
GPS
USB POWER
BATTERY MANAGEMENT
BATTERY
81
83
125
123
75
73
77
76
74
72
78
82
80
84
86
110
116
112
114
106
108
104
102
100
92
98
96
88
90
122
118
120
124
128
94

FIG. 3

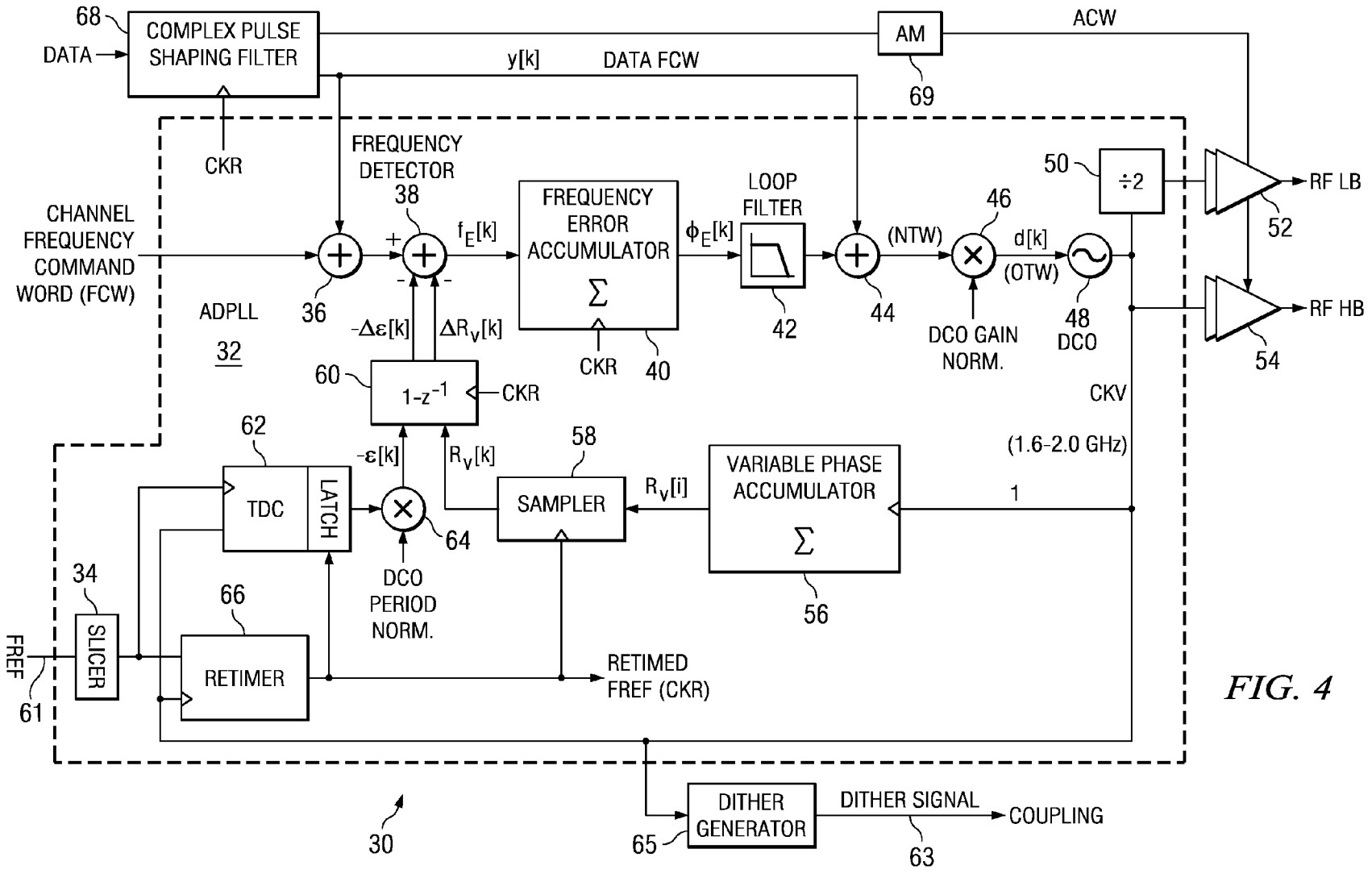

68
COMPLEX PULSE SHAPING FILTER
DATA
CKR
y[k]
DATA FCW
AM
69
ACW
FREQUENCY DETECTOR
38
CHANNEL FREQUENCY COMMAND WORD (FCW)
ADPLL
32
36
+
-
-
$f_E[k]$
FREQUENCY ERROR ACCUMULATOR
Σ
CKR
40
$\phi_E[k]$
LOOP FILTER
42
44
(NTW)
46
DCO GAIN NORM.
d[k]
(OTW)
48
DCO
50
÷2
RF LB
52
RF HB
54
CKV
(1.6-2.0 GHz)
$-\Delta\varepsilon[k]$
$\Delta R_V[k]$
60
$1-z^{-1}$
CKR
62
TDC
LATCH
$-\varepsilon[k]$
$R_V[k]$
58
SAMPLER
$R_V[i]$
VARIABLE PHASE ACCUMULATOR
Σ
56
1
64
DCO PERIOD NORM.
34
SLICER
66
RETIMER
FREF
61
RETIMED FREF (CKR)
30
65
DITHER GENERATOR
DITHER SIGNAL
63
COUPLING

FIG. 4

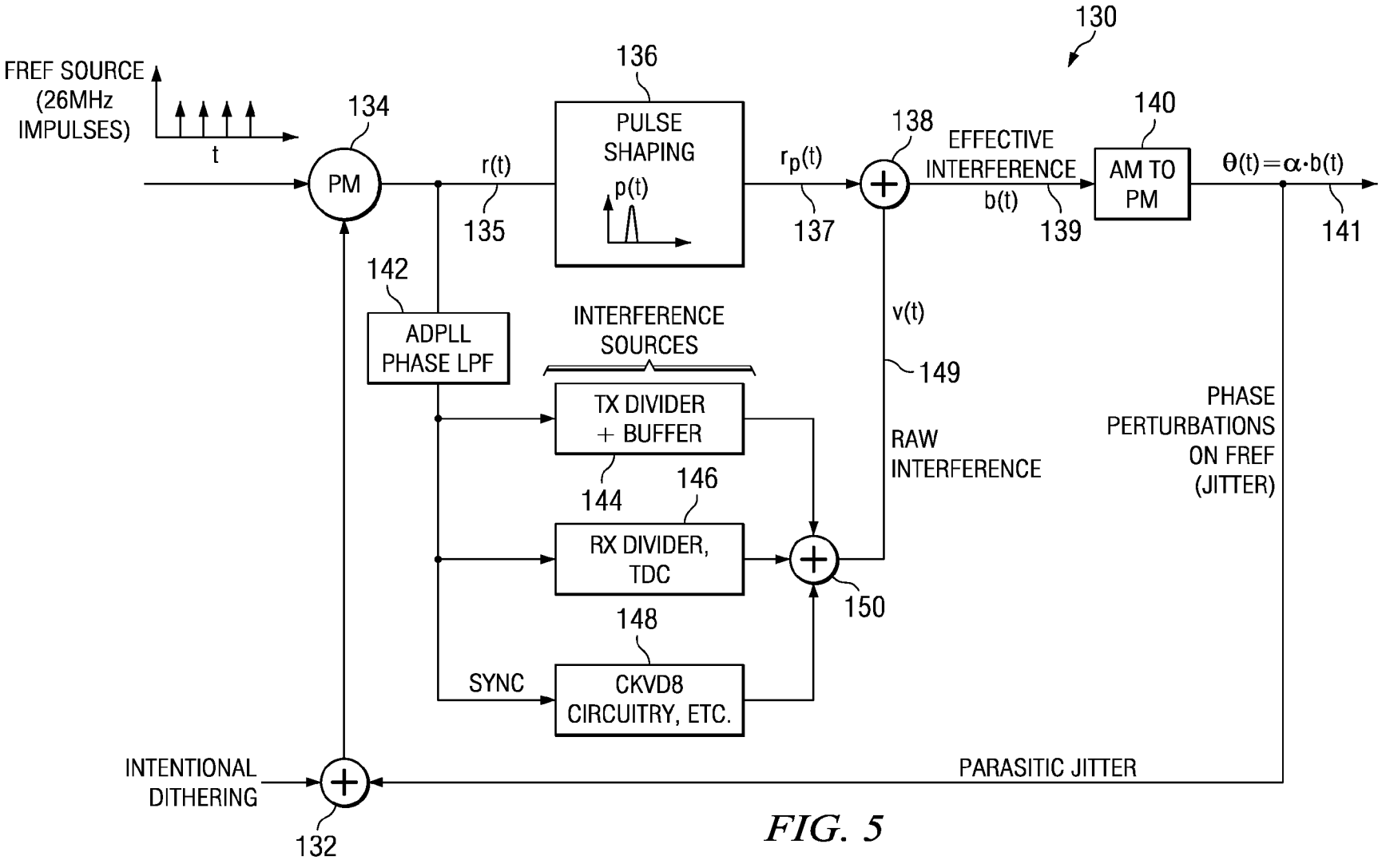

130
FREF SOURCE
(26MHz
IMPULSES)
t
134
PM
136
PULSE
SHAPING
p(t)
r(t)
135
$r_p(t)$
137
138
EFFECTIVE
INTERFERENCE
b(t)
139
140
AM TO
PM
$\theta(t)=\alpha \cdot b(t)$
141
142
ADPLL
PHASE LPF
INTERFERENCE
SOURCES
v(t)
149
TX DIVIDER
+ BUFFER
144
146
RX DIVIDER,
TDC
150
148
SYNC
CKVD8
CIRCUITRY, ETC.
RAW
INTERFERENCE
PHASE
PERTURBATIONS
ON FREF
(JITTER)
INTENTIONAL
DITHERING
132
PARASITIC JITTER

FIG. 5

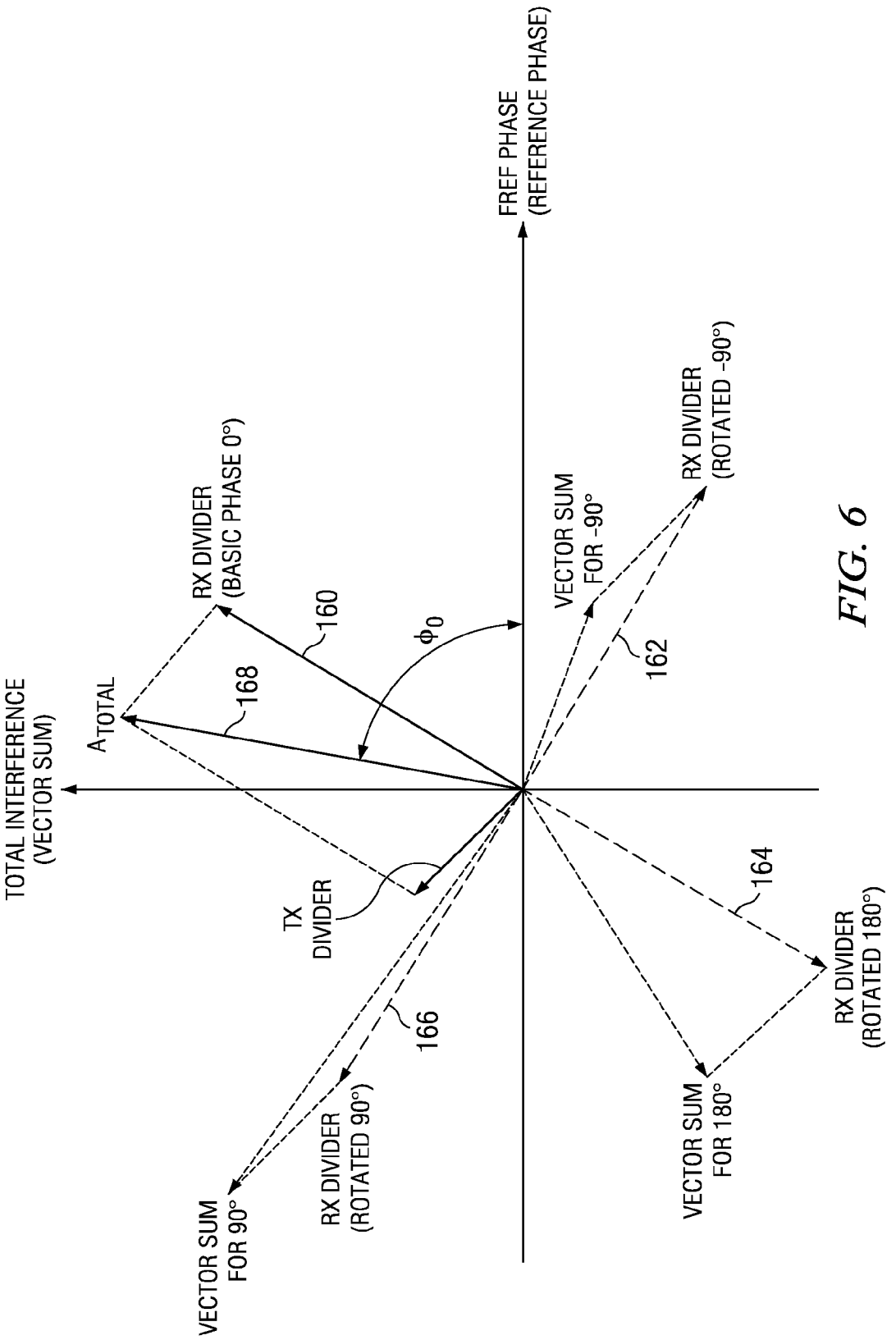

FREF PHASE
(REFERENCE PHASE)
RX DIVIDER
(BASIC PHASE 0°)
160
ϕ_0
VECTOR SUM
FOR -90°
RX DIVIDER
(ROTATED -90°)
162
TOTAL INTERFERENCE
(VECTOR SUM)
A_{TOTAL}
168
TX
DIVIDER
164
RX DIVIDER
(ROTATED 180°)
166
VECTOR SUM
FOR 90°
RX DIVIDER
(ROTATED 90°)
VECTOR SUM
FOR 180°

FIG. 6

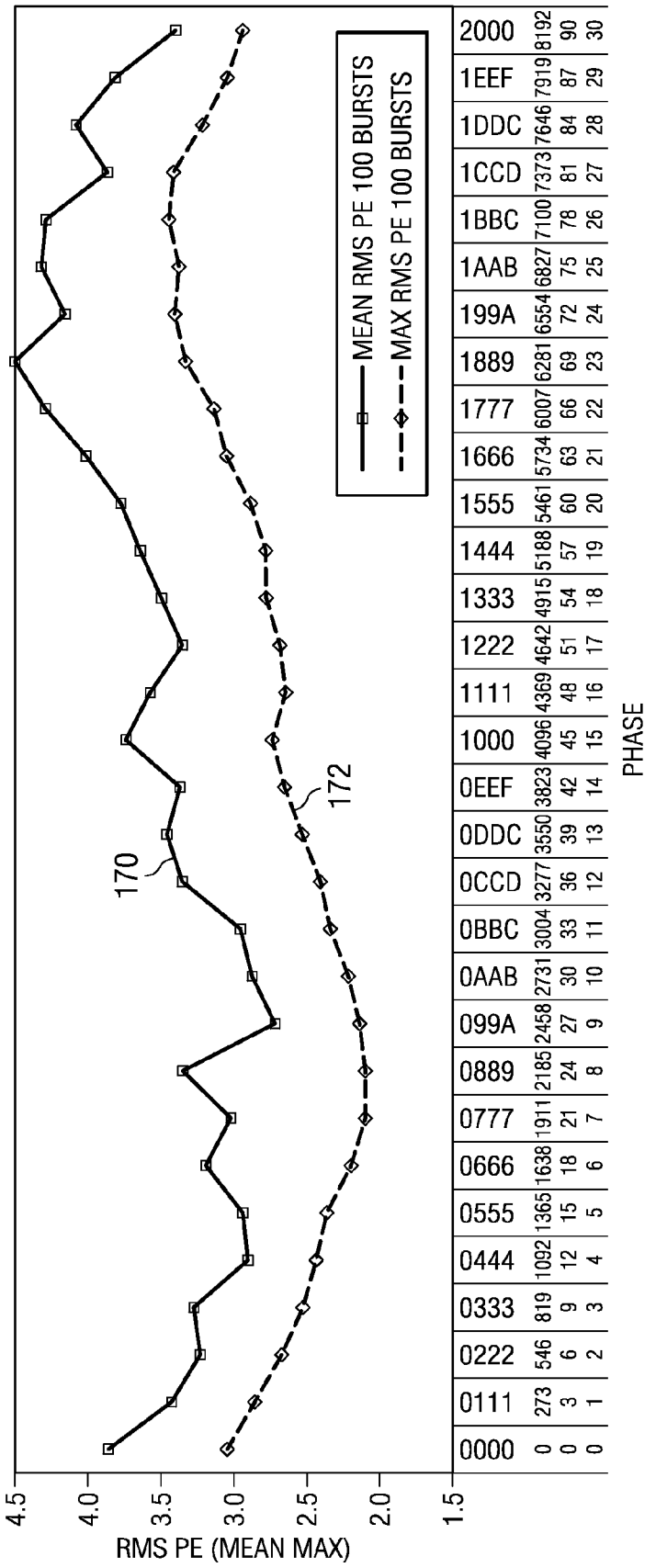
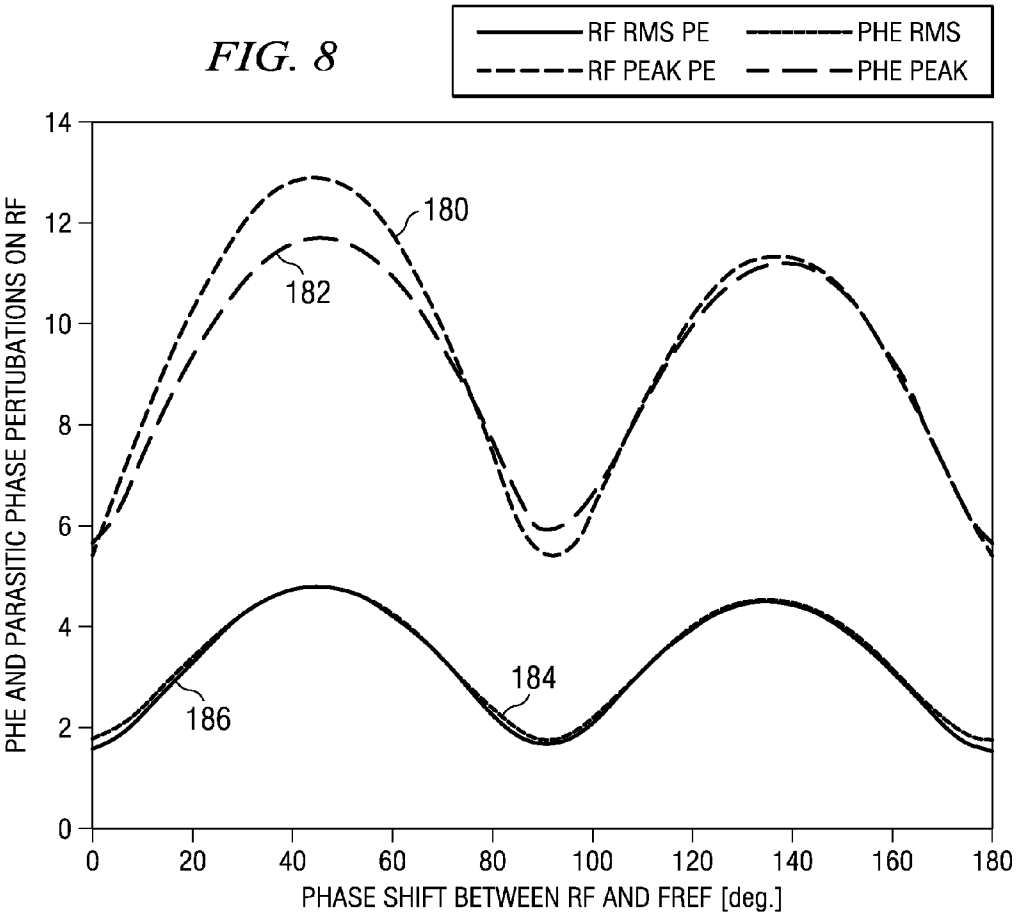

MEAN RMS PE 100 BURSTS
MAX RMS PE 100 BURSTS
170
172
RMS PE (MEAN MAX)
4.5
4.0
3.5
3.0
2.5
2.0
1.5
PHASE
0000 0 0 0
0111 273 3 1
0222 546 6 2
0333 819 9 3
0444 1092 12 4
0555 1365 15 5
0666 1638 18 6
0777 1911 21 7
0889 2185 24 8
099A 2458 27 9
0AAB 2731 30 10
0BBC 3004 33 11
0CCD 3277 36 12
0DDC 3550 39 13
0EEF 3823 42 14
1000 4096 45 15
1111 4369 48 16
1222 4642 51 17
1333 4915 54 18
1444 5188 57 19
1555 5461 60 20
1666 5734 63 21
1777 6007 66 22
1889 6281 69 23
199A 6554 72 24
1AAB 6827 75 25
1BBC 7100 78 26
1CCD 7373 81 27
1DDC 7646 84 28
1EEF 7919 87 29
2000 8192 90 30

FIG. 7

FIG. 8


RF RMS PE
PHE RMS
RF PEAK PE
PHE PEAK
PHE AND PARASITIC PHASE PERTUBATIONS ON RF
PHASE SHIFT BETWEEN RF AND FREF [deg.]
180
182
184
186
0
2
4
6
8
10
12
14
0
20
40
60
80
100
120
140
160
180

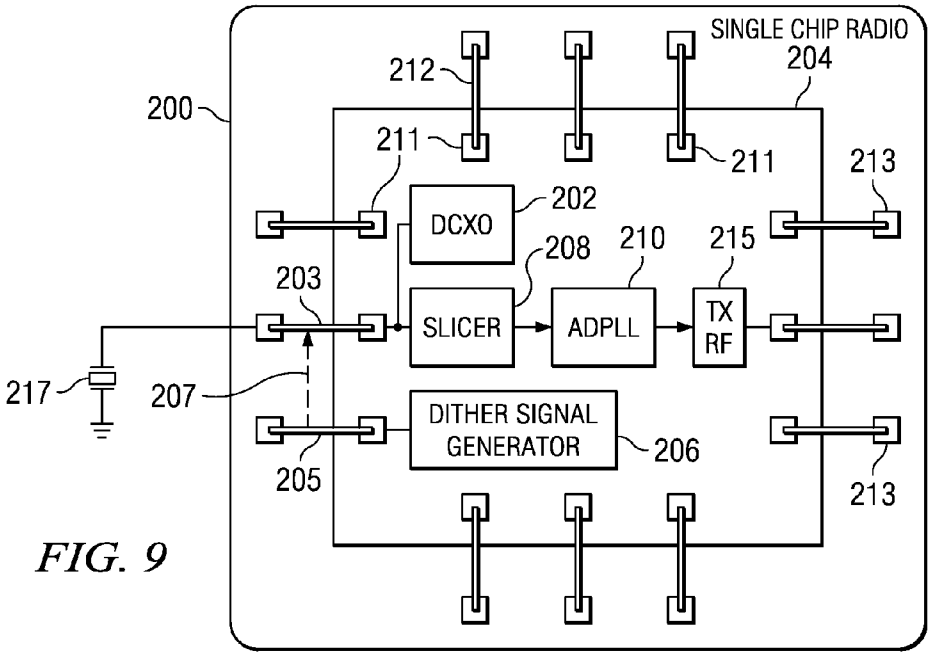

SINGLE CHIP RADIO
204
200
212
211
211
213
DCXO
202
208
210
215
203
SLICER
ADPLL
TX
RF
217
207
DITHER SIGNAL
GENERATOR
206
205
213

FIG. 9

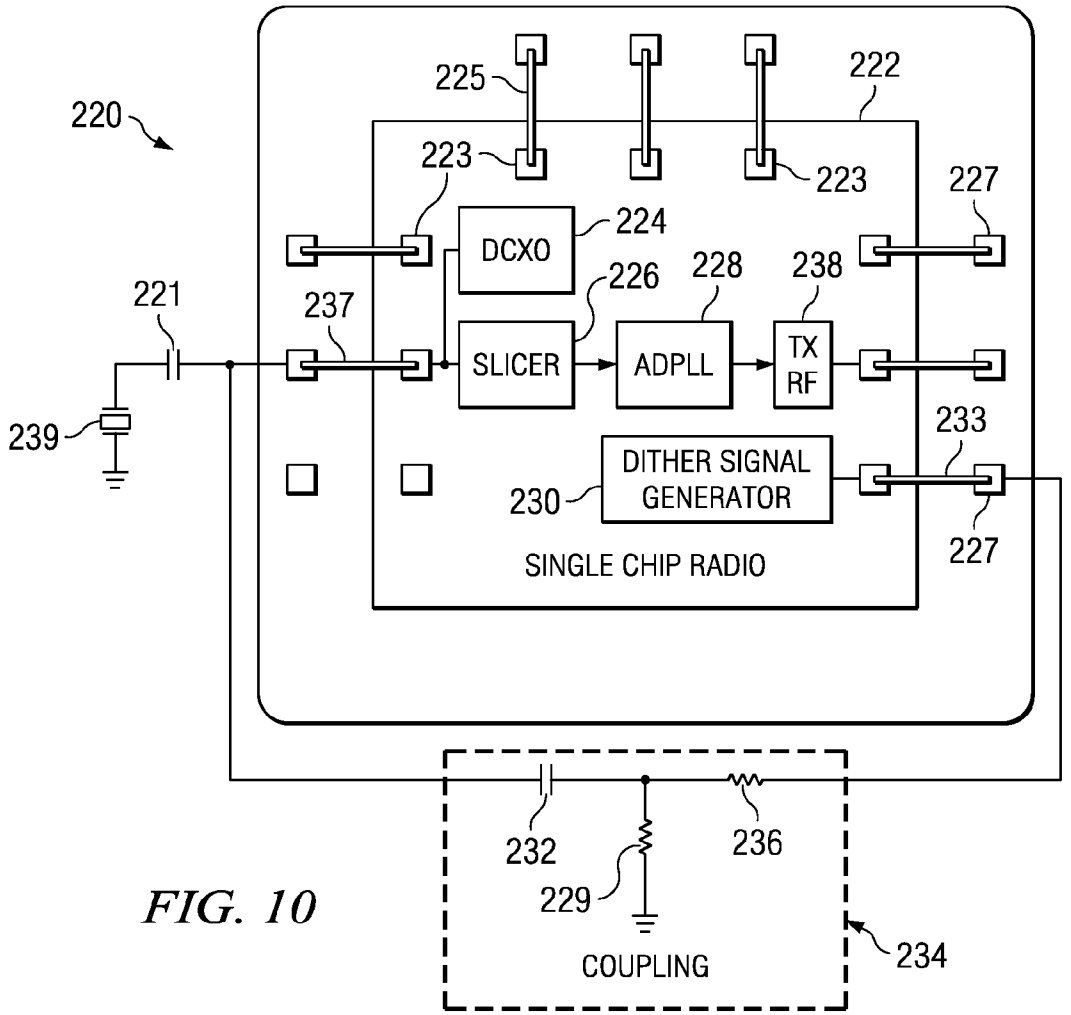

220
225
222
223
223
227
DCXO
224
226
228
238
221
237
SLICER
ADPLL
TX
RF
239
233
DITHER SIGNAL
GENERATOR
230
227
SINGLE CHIP RADIO
232
236
229
COUPLING
234

FIG. 10

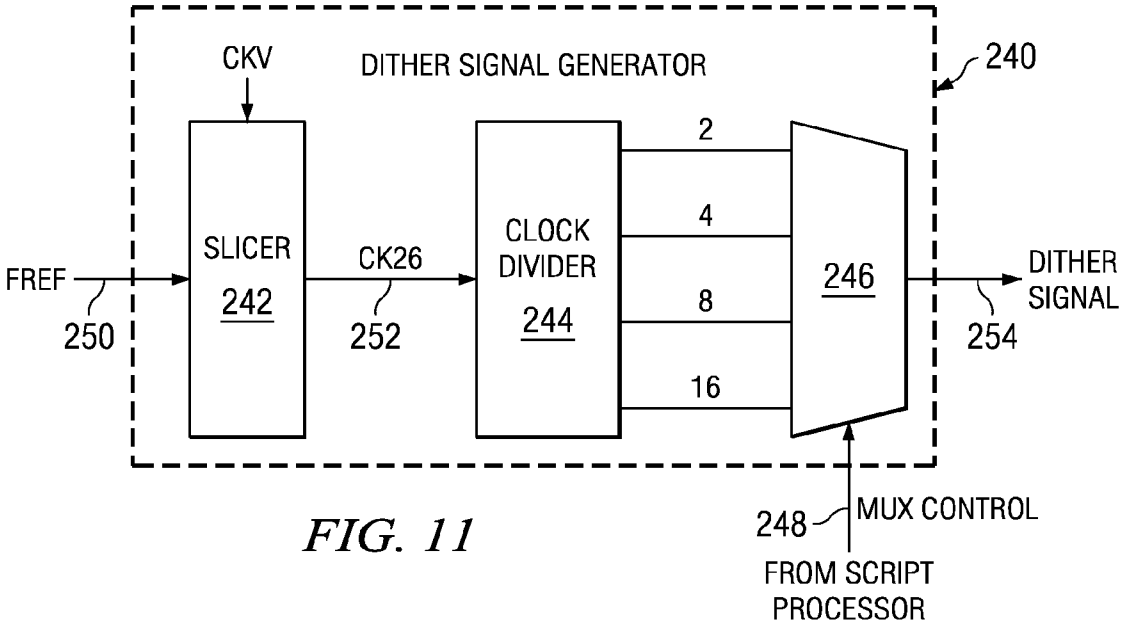

CKV
DITHER SIGNAL GENERATOR
240
2
4
8
16
SLICER
242
CK26
CLOCK
DIVIDER
244
246
FREF
250
252
DITHER
SIGNAL
254
248
MUX CONTROL
FROM SCRIPT
PROCESSOR

FIG. 11

MINIMIZATION OF RMS PHASE ERROR IN A PHASE LOCKED LOOP BY DITHERING OF A FREQUENCY REFERENCE

REFERENCE TO PRIORITY APPLICATION

[0001] This application claims priority to U.S. Provisional Application Ser. No. 60/889,334, filed Feb. 12, 2007, entitled "Dithering of Frequency Reference Through Bond Wires", incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

[0002] The present invention relates to the field of data communications and more particularly relates to an apparatus for and method of minimizing the root mean squared (RMS) phase error in a phase locked loop (PLL) by dithering of a frequency reference.

BACKGROUND OF THE INVENTION

[0003] A diagram illustrating an example prior art single chip polar transceiver radio incorporating an all digital phase locked loop (ADPLL) based transmitter is shown in FIG. **1**. The single chip radio, generally referenced **10**, comprises an ADPLL circuit **16**, pulse shaper **12**, amplitude modulation (AM) circuit **14**, digital RF to amplitude converter (DRAC) **18** which consists of a Pre Power Amplifier (PPA) and Sigma-Delta Amplitude Modulator (SAM), digitally controlled crystal oscillator (DCXO) **20** and slicer **25**.

[0004] The radio implements a direct FM or polar transmitter whereby the ADPLL generates an output frequency in accordance with a frequency control word (FCW) input. The CKV clock signal output of the ADPLL is amplitude modulated in accordance with an amplitude control word (ACW) generated by the AM circuit **14**.

[0005] Depending on the particular implementation of the radio, a potential problem that may occur is excessive RMS phase error, or phase/frequency modulation distortion in general, for "integer channels" of transmission. The integer channels are those for which the ratio between the carrier frequency produced by the ADPLL (or the LO frequency, which may be at 2× the carrier frequency) is an integer multiple of the input reference frequency FREF. More specifically, the RMS phase error problem is due to the RF output or internal RF (e.g., digital RF) signal coupling back into the DCXO that provides the frequency reference signal for the local oscillator based on the ADPLL. The much higher frequency RF output signal that is generated is coupled into the much lower frequency FREF input, where a slicer exists to convert the oscillations into a two-level clock signal. This slicer, typically based on a comparator (open loop of positive feedback amplifier), performs a non-linear operation which allows the additive interference to translate into additive phase (or jitter) on the clock produced by this circuit. It is noted that this problem can arise in any type of PLL or frequency synthesizer circuit, where the output RF signal has the opportunity of coupling into the FREF circuitry, as typically is the case in a system-on-chip (SoC) environment.

[0006] The coupling mechanism is modeled in FIG. **1** as a modulus CKV/FREF block **26** coupled to a gain block **24**. This interference signal is coupled to the FREF signal via virtual adder **22** before it enters the slicer **25**. Thus, the frequency reference signal output of the slicer contains this interference signal. Thus, the ADPLL output, derived signals or the RF output signal is effectively coupled (various paths are indicated by dotted lines **28** and **29**) from the output of the transmitter back to the frequency reference input.

[0007] In highly integrated small silicon area radios, such as radios with integrated RF and digital baseband (DBB), with very short separation between the RF and FREF bond pads, bond wires, balls and pins, this problem is practically unavoidable.

[0008] There is thus a need for a mechanism that is capable of mitigating or eliminating the effects of the interference caused by coupling of the transmit RF output signal, or internal signals derived from it, back into the frequency reference input to the ADPLL based local oscillator.

SUMMARY OF THE INVENTION

[0009] The present invention is a novel and useful apparatus for and method of minimizing the root mean squared (RMS) phase error, or phase/frequency distortions in general, in a phase locked loop (PLL) by dithering of its frequency reference. The dithering of the frequency reference can be accomplished via (1) indirect coupling via bond wires (i.e. package parasitics) or (2) direct coupling via coupling circuitry. The frequency reference dithering mechanism of the present invention is operative to dither the DCXO buffer signal in a controlled manner by utilizing bond wire or direct coupling. The available oscillator clock is divided by power of two or other ratio into a multiplexer. The dither signal is generated by switching between two or more of the clock signal generated. The control of the multiplexer may be performed by any control entity such as an onboard script processor.

[0010] The dither signal is coupled through a bond wire sufficiently close in proximity to the frequency reference circuit input or direct coupling. In general, the frequency reference circuit can be dithered with any clock signal, by varying its threshold voltage in the associated slicer circuit. This desensitizes the RF signal conversion into frequency reference timestamp deviations by applying a strong but periodical stimulus.

[0011] The invention is applicable to single chip radios that integrate the RF circuitry with the digital base band (DBB) circuitry on the same die or on close proximity thereto so as to exhibit interference from the transmit RF output signal coupling back into the frequency reference input. In a single chip radio, the reference frequency circuit area with its associated bond pads, bond wires, etc. is very close to the VCO and RF output buffers and their associated bond pads and wires.

[0012] Advantages of the reference frequency dithering mechanism include (1) providing a solution to mitigate the interference (i.e. unacceptable levels of RMS phase error) caused by coupling of the transmit RF output signal into the frequency reference input; (2) implementation of the mechanism should not normally require any silicon re-work for existing single chip radio designs; and (3) if controllable coupling is required, its costs and complexity are extremely low.

[0013] Note that some aspects of the invention described herein may be constructed as software objects that are executed in embedded devices as firmware, software objects that are executed as part of a software application on either an embedded or non-embedded computer system such as a digital signal processor (DSP), microcomputer, minicomputer, microprocessor, etc running a real-time operating system such as WinCE, Symbian, OSE, Embedded LINUX, etc. or non-real time operating system such as Windows, UNIX,

LINUX, etc., or as soft core realized HDL circuits embodied in an Application. Specific Integrated Circuit (ASIC) or Field Programmable Gate Array (FPGA), or as functionally equivalent discrete hardware components.

[0014] There is thus provided in accordance with the present invention, a method of minimizing the impact of interference to a frequency reference input from a radio frequency (RF) signal, the method comprising the steps of generating a dithering signal and coupling the dithering signal to the frequency reference input to generate a modulated frequency reference signal modulated with the dithering signal.

[0015] There is also provided in accordance with the present invention, a method of minimizing the impact of a transmit radio frequency (RF) signal interference signal on a frequency reference input, the method comprising the steps of generating a periodical stimulus signal, coupling the periodical stimulus signal to the frequency reference input and frequency modulating the frequency reference input wherein the spectral content of the transmit RF interference signal is substantially shifted outside a particular frequency band of interest.

[0016] There is further provided in accordance with the present invention, a phase locked loop (PLL) comprising a frequency reference input, a radio frequency (RF) output having a frequency in accordance with the frequency reference input and a frequency command signal, a slicer coupled to the frequency reference input, the slicer operative to digitize a signal input thereto, means for generating a dithering signal and coupling means for coupling the dithering signal to the slicer, wherein the coupling means is operative to reduce the effect of interference caused by the RF output on the frequency reference input.

[0017] There is also provided in accordance with the present invention, a single chip radio comprising a polar transmitter, the transmitter comprising a phase locked loop (PLL), the phase locked loop comprising a frequency reference input, a radio frequency (RF) output having a frequency in accordance with the frequency reference input and a frequency command signal, a slicer coupled to the frequency reference input, the slicer operative to digitize a signal input thereto, means for generating a dithering signal, coupling means for coupling the dithering signal to the frequency reference input, wherein the coupling means is operative to reduce the effect of interference caused by the RF output on the frequency reference input, a receiver and a baseband processor coupled to the transmitter and the receiver.

[0018] There is further provided in accordance with the present invention, a mobile communications device comprising a cellular radio comprising a transmitter and receiver, the transmitter comprising a phase locked loop (PLL), the phase locked loop comprising a frequency reference input, a radio frequency (RF) output having a frequency in accordance with the frequency reference input and a frequency command signal, a slicer coupled to the frequency reference input, the slicer operative to digitize a signal input thereto, means for generating a dithering signal, coupling means for coupling the dithering signal to the frequency reference input, wherein the coupling means is operative to reduce the effect of interference caused by the RF output on the frequency reference input and a processor coupled to the transmitter and receiver.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The invention is herein described, by way of example only, with reference to the accompanying drawings, wherein:

[0020] FIG. **1** is a diagram illustrating an example prior art single chip polar transceiver radio showing a transmitter incorporating an all digital phase locked loop (ADPLL) based transmitter circuits, as well as the potential parasitic coupling paths;

[0021] FIG. **2**A is a block diagram illustrating a single chip polar transceiver radio incorporating an all-digital local oscillator based transmitter and receiver and indirect coupling frequency reference dithering mechanism of the present invention;

[0022] FIG. **2**B is a block diagram illustrating a single chip polar transceiver radio incorporating an all-digital local oscillator based transmitter and receiver and direct coupling frequency reference dithering mechanism of the present invention;

[0023] FIG. **3** is a simplified block diagram illustrating an example mobile communication device incorporating the frequency reference dithering mechanism of the present invention;

[0024] FIG. **4** is a block diagram illustrating an example ADPLL incorporating the frequency reference dithering mechanism of the present invention;

[0025] FIG. **5** is an equivalent block of the general interference mechanism model;

[0026] FIG. **6** is a vector diagram for multiple interference sources at the second harmonic;

[0027] FIG. **7** is a graph illustrating the periodic characterization of the phase dependency;

[0028] FIG. **8** is a graph illustrating the RMS and peak of interference and proportional jitter versus RF/FREF phase shift of an integer-N channel;

[0029] FIG. **9** is a diagram illustrating an example single chip radio incorporating a first embodiment of the frequency reference dithering mechanism of the present invention;

[0030] FIG. **10** is a diagram illustrating an example single chip radio incorporating a second embodiment of the frequency reference dithering mechanism of the present invention; and

[0031] FIG. **11** is a block diagram illustrating the dither signal generator of the present invention in more detail.

DETAILED DESCRIPTION OF THE INVENTION

Notation Used Throughout

[0032] The following notation is used throughout this document.

Term	Definition
AC	Alternating Current
ACW	Amplitude Control Word
ADC	Analog to Digital Converter
ADPLL	All Digital Phase Locked Loop
AM	Amplitude Modulation
ASIC	Application Specific Integrated Circuit
AVI	Audio Video Interface
BIST	Built-In Self Test
BMP	Windows Bitmap
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DBB	Digital Baseband
DC	Direct Current
DCO	Digitally Controlled Oscillator
DCXO	Digitally Controlled Crystal Oscillator
DPA	Digitally Controlled Power Amplifier

-continued

Term	Definition
DRAC	Digital to RF Amplitude Conversion
DRP	Digital RF Processor or Digital Radio Processor
DSL	Digital Subscriber Line
DSP	Digital Signal Processor
EDGE	Enhanced Data Rates for GSM Evolution
EDR	Enhanced Data Rate
EPROM	Erasable Programmable Read Only Memory
FCW	Frequency Command Word
FIB	Focused Ion Beam
FM	Frequency Modulation
FPGA	Field Programmable Gate Array
GMSK	Gaussian Minimum Shift Keying
GPS	Global Positioning System
GSM	Global System for Mobile communications
HB	High Band
HDL	Hardware Description Language
IEEE	Institute of Electrical and Electronics Engineers
IIR	Infinite Impulse Response
JPG	Joint Photographic Experts Group
LAN	Local Area Network
LB	Low Band
LDO	Low Drop Out
LO	Local Oscillator
MBOA	Multiband OFDM Alliance
MIM	Metal Insulator Metal
MOS	Metal Oxide Semiconductor
MP3	MPEG-1 Audio Layer 3
MPG	Moving Picture Experts Group
PA	Power Amplifier
PC	Personal Computer
PDA	Personal Digital Assistant
PHE	Phase Error
PLL	Phase Locked Loop
PM	Phase Modulation
PPA	Pre-Power Amplifier
RAM	Random Access Memory
RF	Radio Frequency
RFBIST	RF Built-In Self Test
RMS	Root Mean Squared
ROM	Read Only Memory
SAM	Sigma-Delta Amplitude Modulation
SAW	Surface Acoustic Wave
SIM	Subscriber Identity Module
SoC	System on Chip
SRAM	Static Read Only Memory
TDC	Time to Digital Converter
TV	Television
USB	Universal Serial Bus
UWB	Ultra Wideband
VCO	Voltage Controlled Oscillator
WCDMA	Wideband Code Division Multiple Access
WiFi	Wireless Fidelity
WiMAX	Worldwide Interoperability for Microwave Access
WiMedia	Radio platform for UWB
WLAN	Wireless Local Area Network
WMA	Windows Media Audio
WMV	Windows Media Video
WPAN	Wireless Personal Area Network

DETAILED DESCRIPTION OF THE INVENTION

[0033] The present invention is a novel and useful apparatus for and method of minimizing the root mean squared (RMS) phase error in a phase locked loop (PLL) by dithering of a frequency reference either via (1) indirect coupling through bond wires (i.e. package parasitics) or (2) direct coupling via coupling circuitry. The frequency reference dithering mechanism of the present invention is operative to dither the DCXO buffer signal in a controlled manner by utilizing bond wire or direct coupling. The available oscillator clock is divided by power of two or other ratio into a multiplexer. The dither signal is generated by switching between two or more of the clock signal generated. The control of the multiplexer may be performed by any control entity such as an onboard script processor.

[0034] Although the frequency reference dithering mechanism is applicable to numerous wireless communication standards and can be incorporated in numerous types of wireless or wired communication devices such a multimedia player, mobile station, cellular phone, PDA, DSL modem, WPAN device, etc., it is described in the context of a digital RF processor (DRP) based transmitter that may be adapted to comply with a particular wireless communications standard such as GSM, Bluetooth, EDGE, WCDMA, WLAN, WiMax, etc. It is appreciated, however, that the invention is not limited to use with any particular communication standard and may be used in optical, wired and wireless applications. Further, the invention is not limited to use with a specific modulation scheme but is applicable to any modulation scheme including both digital and analog modulations where there is a need to mitigate the interference affects of the coupling of the transmit RF output signal back into the frequency reference input.

[0035] Note that throughout this document, the term communications device is defined as any apparatus or mechanism adapted to transmit, receive or transmit and receive data through a medium. The term communications transceiver or communications device is defined as any apparatus or mechanism adapted to transmit and receive data through a medium. The communications device or communications transceiver may be adapted to communicate over any suitable medium, including wireless or wired media. Examples of wireless media include RF, infrared, optical, microwave, UWB, Bluetooth, WiMAX, WiMedia, WiFi, or any other broadband medium, etc. Examples of wired media include twisted pair, coaxial, optical fiber, any wired interface (e.g., USB, Firewire, Ethernet, etc.). The term Ethernet network is defined as a network compatible with any of the IEEE 802.3 Ethernet standards, including but not limited to 10Base-T, 100Base-T or 1000Base-T over shielded or unshielded twisted pair wiring. The terms communications channel, link and cable are used interchangeably. The notation DRP is intended to denote either a Digital RF Processor or Digital Radio Processor. References to a Digital RF Processor infer a reference to a Digital Radio Processor and vice versa.

[0036] The term multimedia player or device is defined as any apparatus having a display screen and user input means that is capable of playing audio (e.g., MP3, WMA, etc.), video (AVI, MPG, WMV, etc.) and/or pictures (JPG, BMP, etc.). The user input means is typically formed of one or more manually operated switches, buttons, wheels or other user input means. Examples of multimedia devices include pocket sized personal digital assistants (PDAs), personal media player/recorders, cellular telephones, handheld devices, and the like.

[0037] Some portions of the detailed descriptions which follow are presented in terms of procedures, logic blocks, processing, steps, and other symbolic representations of operations on data bits within a computer memory. These descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. A procedure, logic block, process, etc., is generally conceived to be a self-consistent sequence of steps or instructions leading to a desired result. The steps require physical manipulations of physical quantities. Usually, though not necessarily,

these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared and otherwise manipulated in a computer system. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, bytes, words, values, elements, symbols, characters, terms, numbers, or the like.

[0038] It should be born in mind that all of the above and similar terms are to be associated with the appropriate physical quantities they represent and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the following discussions, it is appreciated that throughout the present invention, discussions utilizing terms such as 'processing,' 'computing,' 'calculating,' 'determining,' 'displaying' or the like, refer to the action and processes of a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

[0039] The invention can take the form of an entirely hardware embodiment, an entirely software embodiment or an embodiment containing a combination of hardware and software elements. In one embodiment, a portion of the mechanism of the invention is implemented in software, which includes but is not limited to firmware, resident software, object code, assembly code, microcode, etc.

[0040] Furthermore, the invention can take the form of a computer program product accessible from a computer-usable or computer-readable medium providing program code for use by or in connection with a computer or any instruction execution system. For the purposes of this description, a computer-usable or computer readable medium is any apparatus that can contain, store, communicate, propagate, or transport the program for use by or in connection with the instruction execution system, apparatus, or device, e.g., floppy disks, removable hard drives, computer files comprising source code or object code, flash semiconductor memory (USB flash drives, etc.), ROM, EPROM, or other semiconductor memory devices.

Single Chip Radio

[0041] A block diagram illustrating a single chip polar transceiver radio incorporating an all-digital local oscillator based transmitter and receiver and indirect coupling frequency reference dithering mechanism of the present invention is shown in FIG. **2**A. For illustration purposes only, the transmitter, as shown, is adapted for the GSM/EDGE/WCDMA cellular standards. It is appreciated, however, that one skilled in the communication arts can adapt the transmitter illustrated herein to other modulations and communication standards as well without departing from the spirit and scope of the present invention.

[0042] The radio circuit, generally referenced **261**, comprises radio integrated circuit coupled to a crystal **280**, front end module **302** and battery management circuit **262**. The radio chip **261** comprises a script processor **274**, digital baseband (DBB) processor **272**, memory **270** (e.g., static RAM), TX block **278**, RX block **276**, crystal **280** and digitally controlled crystal oscillator (DCXO) **290**, slicer **291**, front-end module **302** and antenna **304**, power management unit **266**, RF built-in self test (BIST) **268**, battery **264** and battery management circuit **262**. The TX block comprises high speed and low speed digital logic block **316** including ΣΔ modulators **292**, **294**, digitally controlled oscillator (DCO) **296** and digitally controlled power amplifier (DPA) **300** or pre power amplifier (PPA). The ADPLL and transmitter generate various radio frequency signals. The RX block comprises a low noise transconductance amplifier **306**, current sampler **308**, discrete time processing block **310**, analog to digital converter (ADC) **312** and digital logic block **314**.

[0043] In accordance with the invention, the radio also comprises a dither signal generator block **282** that is operative to generate a dither signal that is routed to a bond wire **284** in close enough physical proximity to the bond wire connecting the crystal **280** to the DCXO **290** to permit coupling (indicated by dotted line **288**) of the dither signal onto the FREF clock signal output of the DCXO and slicer **291**. It is noted that the frequency reference dithering mechanism (both indirect and direct) is applicable to any type of PLL or frequency synthesizer. In addition, the clock input to the dither signal generator circuit may comprise any desired clock signal, e.g., FREF, CKV, etc.

[0044] The principles presented herein have been used to develop three generations of a Digital RF Processor (DRP): single-chip Bluetooth, GSM and GSM/EDGE radios realized in 130 nm, 90 nm and 65 nm digital CMOS process technologies, respectively. The common architecture is highlighted in FIG. **2**A with features added specific to the cellular radio. The all digital phase locked loop (ADPLL) based transmitter employs a polar architecture with all digital phase/frequency and amplitude modulation paths. The receiver employs a discrete-time architecture in which the RF signal is directly sampled and processed using analog and digital signal processing techniques.

[0045] A key component is the digitally controlled oscillator (DCO) **296**, which avoids any analog tuning controls. A digitally-controlled crystal oscillator (DCXO) generates a high-quality base station-synchronized frequency reference such that the transmitted carrier frequencies and the received symbol rates are accurate to within 0.1 ppm. Fine frequency resolution is achieved through high-speed ΣΔ dithering of its varactors. Digital logic built around the DCO realizes an all-digital PLL (ADPLL) that is used as a local oscillator for both the transmitter and receiver. The polar transmitter architecture utilizes the wideband direct frequency modulation capability of the ADPLL and a digitally controlled power amplifier (DPA) **300** for the amplitude modulation. The DPA operates in near-class-E mode and uses an array of nMOS transistor switches to regulate the RF amplitude and acts as a digital-to-RF amplitude converter (DRAC). It is followed by a matching network and an external front-end module **302**, which comprises a power amplifier (PA), a transmit/receive switch for the common antenna **304** and RX surface acoustic wave (SAW) filters. Fine amplitude resolution is achieved through high-speed ΣΔ dithering of the DPA nMOS transistors.

[0046] The receiver **276** employs a discrete-time architecture in which the RF signal is directly sampled at the Nyquist rate of the RF carrier and processed using analog and digital signal processing techniques. The transceiver is integrated with a script processor **274**, dedicated digital base band processor **272** (i.e. ARM family processor or DSP) and SRAM memory **270**. The script processor handles various TX and RX calibration, compensation, sequencing and lower-rate

data path tasks and encapsulates the transceiver complexity in order to present a much simpler software programming model.

[0047] The frequency reference (FREF) is generated on-chip by a 26 MHz (could be 38.4 MHz or other) digitally controlled crystal oscillator (DCXO) **290** coupled to slicer **291**. An integrated power management (PM) system is connected to an external battery management circuit **262** that conditions and stabilizes the supply voltage. The PM comprises multiple low drop out (LDO) regulators that provide internal supply voltages and also isolate supply noise between circuits, especially protecting the DCO. The RF built-in self-test (RFBIST) **268** performs autonomous phase noise and modulation distortion testing, various loopback configurations for bit-error rate measurements and implements the DPA calibration and BIST mechanism of the invention, described in more detail infra. The transceiver is integrated with the digital baseband, SRAM memory in a complete system-on-chip (SoC) solution. Almost all the clocks on this SoC are derived from and are synchronous to the RF oscillator clock. This helps to reduce susceptibility to the noise generated through clocking of the massive digital logic.

[0048] The transmitter comprises a polar architecture in which the amplitude and phase/frequency modulations are implemented in separate paths. Transmitted symbols generated in the digital baseband (DBB) processor are first pulse-shape filtered in the Cartesian coordinate system. The filtered in-phase (I) and quadrature (Q) samples are then converted through a CORDIC algorithm into amplitude and phase samples of the polar coordinate system. The phase is then differentiated to obtain frequency deviation. The polar signals are subsequently conditioned through signal processing to sufficiently increase the sampling rate in order to reduce the quantization noise density and lessen the effects of the modulating spectrum replicas.

[0049] A more detailed description of the operation of the ADPLL can be found in U.S. Patent Publication No. 2006/0033582A1, published Feb. 16, 2006, to Staszewski et al., entitled "Gain Calibration of a Digital Controlled Oscillator," U.S. Patent Publication No. 2006/0038710A1, published Feb. 23, 2006, Staszewski et al., entitled "Hybrid Polar/Cartesian Digital Modulator" and U.S. Pat. No. 6,809,598, to Staszewski et al., entitled "Hybrid Of Predictive And Closed-Loop Phase-Domain Digital PLL Architecture," all of which are incorporated herein by reference in their entirety.

[0050] In a direct coupling embodiment, rather than employ indirect coupling between closely situated bond wires, the invention comprises a direct coupling mechanism whereby the dither signal is coupled to the reference frequency input via coupling circuitry. A block diagram illustrating a single chip polar transceiver radio incorporating an all-digital local oscillator based transmitter and receiver and direct coupling frequency reference dithering mechanism of the present invention is shown in FIG. **2**B.

[0051] The radio circuit, generally referenced **320**, comprises the radio integrated circuit **261** the operation of which is described in detail supra. Note that for clarity sake, only a few internal blocks are shown in FIG. **2**B. In this direct coupling embodiment described herein, however, the de-sensitization of the reference frequency input does not rely on indirect coupling via bond wires. In situations where indirect coupling is not possible or practical, direct coupling is used,

[0052] In this example embodiment, the coupling circuit comprises a high pass RC circuit comprising capacitor **328** and resistors **324**, **326** (forming a voltage divider). The dither signal output of the dither signal generator **282** is input to the RC coupling circuit. The output of the coupling circuit is connected between capacitor crystal **280** and the DCXO **290**.

Mobile Device/Cellular Phone/PDA System

[0053] A simplified block diagram illustrating an example communication device incorporating the frequency reference dithering mechanism of the present invention is shown in FIG. **3**. The communication device may comprise any suitable wired or wireless device such as a multimedia player, mobile station, mobile device, cellular phone, PDA, wireless personal area network (WPAN) device, Bluetooth EDR device, etc. For illustration purposes only, the communication device is shown as a cellular phone or smart phone. Note that this example is not intended to limit the scope of the invention as the frequency reference dither mechanism of the present invention can be implemented in a wide variety of wireless and wired communication devices.

[0054] The cellular phone, generally referenced **70**, comprises a baseband processor or CPU **71** having analog and digital portions. The basic cellular link is provided by the RF transceiver **94** and related one or more antennas **96**, **98**. A plurality of antennas is used to provide antenna diversity which yields improved radio performance. The cell phone also comprises internal RAM and ROM memory **110**, Flash memory **112** and external memory **114**.

[0055] In accordance with the invention, the RF transceiver comprises a dither signal generator **128** operative to mitigate the interference caused by coupling of the transmit RF output signal back into the frequency reference input, as described in more detail infra. In operation, the dither signal generator and related frequency reference dithering mechanism may be implemented as hardware, as software executed as a task on the baseband processor **71** or a combination of hardware and software. Implemented as a software task, the program code operative to implement the frequency reference dithering mechanism of the present invention is stored in one or more memories **110**, **112** or **114**.

[0056] Several user interface devices include microphone **84**, speaker **82** and associated audio codec **80**, a keypad for entering dialing digits **86**, vibrator **88** for alerting a user, camera and related circuitry **100**, a TV tuner **102** and associated antenna **104**, display **106** and associated display controller **108** and GPS receiver **90** and associated antenna **92**.

[0057] A USB interface connection **78** provides a serial link to a user's PC or other device. An FM receiver **72** and antenna **74** provide the user the ability to listen to FM broadcasts. WLAN radio and interface **76** and antenna **77** provide wireless connectivity when in a hot spot or within the range of an ad hoc, infrastructure or mesh based wireless LAN network. A Bluetooth EDR radio and interface **73** and antenna **75** provide Bluetooth wireless connectivity when within the range of a Bluetooth wireless network. Further, the communication device **70** may also comprise a WiMAX radio and interface **123** and antenna **125**. SIM card **116** provides the interface to a user's SIM card for storing user data such as address book entries, etc. The communication device **70** also comprises an Ultra Wideband (UWB) radio and interface **83** and antenna **81**. The UWB radio typically comprises an MBOA-UWB based radio.

[0058] Portable power is provided by the battery **124** coupled to battery management circuitry **122**. External power is provided via USB power **118** or an AC/DC adapter **120** connected to the battery management circuitry which is operative to manage the charging and discharging of the battery **124**.

ADPLL Polar Transmitter Incorporating Frequency Reference Dithering Mechanism

[0059] A block diagram illustrating an ADPLL-based polar transmitter for wireless applications incorporating the frequency reference dithering mechanism of the present invention is shown in FIG. **4**. A more detailed description of the operation of the ADPLL can be found in U.S. Patent Publication No. 2006/0033582A1, published Feb. 16, 2006, to Staszewski et al., entitled "Gain Calibration of a Digital Controlled Oscillator," U.S. Patent Publication No. 2006/0038710A1, published Feb. 23, 2006, Staszewski et al., entitled "Hybrid Polar/Cartesian Digital Modulator" and U.S. Pat. No. 6,809,598, to Staszewski et al., entitled "Hybrid Of Predictive And Closed-Loop Phase-Domain Digital PLL Architecture," all of which are incorporated herein by reference in their entirety.

[0060] For illustration purposes only, the transmitter, as shown, is adapted for the GSM/EDGE/WCDMA cellular standards. It is appreciated, however, that one skilled in the communication arts can adapt the transmitter illustrated herein to other modulations and communication standards as well without departing from the spirit and scope of the present invention.

[0061] The transmitter, generally referenced **30**, is well-suited for a deep-submicron CMOS implementation. The transmitter comprises a complex pulse shaping filter **68**, amplitude modulation (AM) block **69** and ADPLL **32**. The circuit **30** is operative to perform complex modulation in the polar domain in addition to the generation of the local oscillator (LO) signal for the receiver. All clocks in the system are derived directly from this source. Note that the transmitter is constructed using digital techniques that exploit the high speed and high density of the advanced CMOS, while avoiding problems related to voltage headroom. The ADPLL circuit replaces a conventional RF synthesizer architecture (based on a voltage-controlled oscillator (VCO) and a phase/frequency detector and charge-pump combination), with a digitally controlled oscillator (DCO) **48** and a time-to-digital converter (TDC) **62**. All inputs and outputs are digital and some even at multi-GHz frequency.

[0062] The core of the ADPLL is a digitally controlled oscillator (DCO) **48** adapted to generate the RF oscillator clock CKV. The oscillator core (not shown) operates at least twice the 1.6-2.0 GHz high band frequency or at least four times the 0.8-1.0 GHz low band frequency. The output of the DCO is then divided for precise generation of RX quadrature signals, and for use as the transmitter's carrier frequency. The single DCO is shared between transmitter and receiver and is used for both the high frequency bands (HB) and the low frequency bands (LB). In additional to the integer control of the DCO, at least 3-bits of the minimal varactor size used are dedicated for ΣΔ dithering in order to improve frequency resolution. The DCO comprises a plurality of varactor banks, which may be realized as n-poly/n-well inversion type MOS capacitor (MOSCAP) devices or Metal Insulator Metal (MIM) devices that operate in the flat regions of their C-V curves to assist digital control. The output of the DCO is input to the RF high band pre-power amplifier (PPA) **52**. It is also input to the RF low band pre-power amplifier **54** after divide by two via divider **50**.

[0063] The expected variable frequency f_V is related to the reference frequency f_R by the frequency command word (FCW).

$$FCW[k] \equiv \frac{E(f_V[k])}{f_R} \tag{1}$$

The FCW is time variant and is allowed to change with every cycle $T_R=1/f_R$ of the frequency reference clock. With $W_F=24$ the word length of the fractional part of FCW, the ADPLL provides fine frequency control with 1.5 Hz accuracy, according to:

$$\Delta f_{res} = \frac{f_R}{2^{W_F}} \tag{2}$$

The number of integer bits $W_I=8$ has been chosen to fully cover the GSM/EDGE and partial WCDMA band frequency range of $f_V=1{,}600$-$2{,}000$ MHz with an arbitrary reference frequency $f_R \geqq 8$ MHz.

[0064] The ADPLL operates in a digitally-synchronous fixed-point phase domain as follows: The variable phase accumulator **56** determines the variable phase $R_V[i]$ by counting the number of rising clock transitions of the DCO oscillator clock CKV as expressed below.

$$R_V[i] = \sum_{l=0}^{i} 1 \tag{3}$$

The index i indicates the DCO edge activity. The variable phase $R_V[i]$ is sampled via sampler **58** to yield sampled FREF variable phase $R_V[k]$, where k is the index of the FREF edge activity. The sampled FREF variable phase $R_V[k]$ is fixed-point concatenated with the normalized time-to-digital converter (TDC) **62** output $\epsilon[k]$. The TDC measures and quantizes the time differences between the frequency reference FREF and the DCO clock edges. The sampled differentiated (via block **60**) variable phase is subtracted from the frequency command word (FCW) by the digital frequency detector **38**. The frequency error $f_E[k]$ samples

$$f_E[k]=\mathrm{FCW}-[(R_V[k]-\epsilon[k])-(R_V[k-1]-\epsilon[k-1])] \tag{4}$$

are accumulated via the frequency error accumulator **40** to create the phase error $\phi_E[k]$ samples

$$\phi_E[k] = \sum_{l=0}^{k} f_E[k] \tag{5}$$

which are then filtered by a fourth order IIR loop filter **42** and scaled by a proportional loop attenuator α. A parallel feed with coefficient ρ adds an integrated term to create type-II loop characteristics which suppress the DCO flicker noise.

[0065] The IIR filter is a cascade of four single stage filters, each satisfying the following equation:

$$y[k]=(1-\lambda)\cdot y[k-1]+\lambda\cdot x[k] \quad (6)$$

wherein

[0066] x[k] is the current input;

[0067] y[k] is the current output;

[0068] k is the time index;

[0069] λ is the configurable coefficient;

The 4-pole IIR loop filter attenuates the reference and TDC quantization noise with an 80 dB/dec slope, primarily to meet the GSM/EDGE spectral mask requirements at 400 kHz offset. The filtered and scaled phase error samples are then multiplied by the DCO gain K_{DCO} normalization factor $f_R/\hat{K}_{DCO}$ via multiplier **46**, where f_R is the reference frequency and $\hat{K}_{DCO}$ is the DCO gain estimate, to make the loop characteristics and modulation independent from K_{DCO}. The modulating data is injected into two points of the ADPLL for direct frequency modulation, via adders **36** and **44**. A hitless gear-shifting mechanism for the dynamic loop bandwidth control serves to reduce the settling time. It changes the loop attenuator a several times during the frequency locking while adding the $(\alpha_1/\alpha_2-1)\phi_1$ dc offset to the phase error, where indices 1 and 2 denote before and after the event, respectively. Note that $\phi_1=\phi_2$, since the phase is to be continuous.

[0070] The FREF input is resampled by the RF oscillator clock CKV via retimer block **66** which may comprise a flip flop or register clocked by the reference frequency FREF. The resulting retimed clock (CKR) is distributed and used throughout the system. This ensures that the massive digital logic is clocked after the quiet interval of the phase error detection by the TDC. Note that in the example embodiment described herein, the ADPLL is a discrete-time sampled system implemented with all digital components connected with all digital signals.

[0071] In accordance with the invention, the transmitter **30** also comprises a dither signal generator **65** that is operative to produce a dither signal **63** based on the CKV clock. In indirect coupling, the dither signal is routed to a bond wire in close physical proximity to the bond wire connecting the frequency reference crystal oscillator output **61** to the DCXO and slicer **34** in the ADPLL circuit such that the dither signal is coupled to the FREF signal **61** thereby mitigating the impact of the interference of the transmit RF output interference to the frequency reference input. In a direct coupling embodiment, the dither signal is directly coupled to the frequency reference input via an RC coupling circuit. Both the indirect and direct coupling mechanisms are described in more detail infra.

Reference Clock Interference and Mitigation Mechanism

[0072] To aid in understanding the principles of operation of the present invention, a detailed description of the problem and its solution is presented below. In particular, a detailed analysis of the interference to the frequency reference clock and the means for its mitigation is presented.

[0073] The interference suffered by the reference clock (FREF) results in intolerable jitter thereon when the transmitter output frequency is centered at an integer multiple (or close thereof) of the FREF clock. In the worst case, a consequence of this interference is potentially failing to meet specifications for phase-error in bursts or packets transmitted at integer channels, resulting from the excessive FREF noise that is tracked by the ADPLL and exhibits itself on the modulated RF carrier. A mathematical model for the interference mechanism is presented as well as the mathematical analyses explaining the performance improvements that were observed through the frequency reference dithering mechanisms of the present invention.

Properties of the Victim Signal FREF and Related Circuitry

[0074] The reference clock FREF is a square-wave signal nominally tuned within the DCXO to 26 MHz, having rise and fall times in the order of 50 ps. This clock signal is generated within the slicer in the DCXO block, where the sine wave is converted into a square-wave clock. The clock signal is then passed from the VDDX domain to the digital circuitry in the VDD_DIG domain through a 600 μm route. Several possible mechanisms of interference along this signal path could potentially result in its contamination and were investigated through simulations, as well as a series of focused ion beam (FIB) modifications and experiments, as described below.

[0075] First, additive interference induced onto the input signal of any block processing FREF (e.g., originating from a sufficiently strong aggressor and coupled through parasitic capacitances). Such additive noise could possibly be picked up at the input to the slicer, on the 600 μm line leading from the DCXO circuitry to the TDC or within the TDC circuitry itself. Second, Vdd/GND interference resulting from inductive coupling through bond wires, which would modulate the supply lines and equivalently the circuit's threshold. Third, Vdd contamination and ground bounces as a result of the use of a common supply (i.e. current surges on the digital supply that are not sufficiently suppressed by decoupling capacitances).

[0076] All three of the above cases effectively constitute AM-to-PM mechanisms which convert the additive interference to jitter. The block diagram of FIG. **5** is an illustration of the interference model for the FREF signal, which would be generally applicable. The model, generally referenced **130**, comprises a FREF phase modulation source **134**, pulse shaping block **136**, multiplier **138**, AM to PM block **140**, ADPLL model block **142**, adders **132**, **150** and a plurality of interference sources including TX divider/buffer **144**, RX divider **146** and clock divider circuitry **148**.

[0077] The various sources of RF interference are driven by the FREF signal and therefore produce signals that are frequency-synchronized with it. The output of this model is the time domain function $\theta(t)$ representing the parasitic phase perturbations on the FREF signal, which the interference induces through the AM to PM conversion occurring within the FREF circuitry. It is these phase perturbations that cause the transmitter's output phase to deviate from the nominal modulation-phase-trajectory thus failing the limits or targets set forth for phase errors (depending the particular specification).

[0078] Since the ADPLL tracks the phase of the FREF signal, a filtered and amplified form of these phase perturbations appear as additive interference in the transmitter's phase modulation, depending on the spectral properties of the signal $\theta(t)$ and the settings of the ADPLL (e.g., loop dynamics). Contrary to the loop dynamics, there's no freedom in the selection of the amplification factor, as it is dictated by the ratio between the required output carrier frequency and the FREF frequency of 26 MHz. Amongst the channels (e.g., 10 in the case of GSM) that suffer from this phenomenon, this

phase amplification factor varies in the range 66 to 73, i.e. the highest integer channel has about 11% more interference gain.

[0079] For the lowest integer channel the amplification factor is 1716 MHz/26 MHz=66 which is approximately 18.2 dB, while for the highest integer channel the amplification factor is 1898 MHz/26 MHz=73 which is approximately 18.6 dB. It is noted that there may be various additional frequency dependent factors that could result in a difference in the level of interference experienced at the 10 channels of interest, such as the coupling factor through which the RF signal couples into the FREF circuitry.

Potential Sources of Interference (Aggressors)

[0080] The CKV clock signal, being equal in frequency to the carrier frequency in high-band, is not the only potential source of interference, since there are several derivatives of it which serve to clock high-speed circuitry, such as CKVD8 (⅛ of the frequency of CKV). It has also been observed that the choice of the Script Processor clock, derived from CKV, has an effect on the transmitter phase-error performance.

[0081] Depending on the particular integer-N channel (i.e. if the ratio is an integer or substantially an integer), each of these derivatives of CKV could be "met" by an appropriately high harmonic of FREF that would down-convert it to zero, where it potentially creates low-frequency jitter on FREF. It is noted that in the absence of modulation (and phase noise), the CKV signal and its derivatives would, theoretically, only create a fixed phase shift in FREF, since their interference at the zero crossing instances (the sampling instances in the model of FIG. **5**) would be the same at each sampling instance (equivalent to a DC shift in the FREF threshold). With modulation present, the various sources of interference, appearing at different multiples of FREF, do not represent the same interference, as the different frequency deviation on each of them would create a different signal once down-converted to zero by the appropriate FREF harmonic in the sampling operation.

[0082] For example, if the CKV signal were to be modulated with all ones (i.e. a fixed carrier frequency shift of about 68 kHz), the CKVD8 clock derivative would have a frequency shift of only 68/8=8.5 kHz from the nominal value of CKVD8=FREF×N/8. Consequently, the down conversion created by the FREF×N/8 harmonic (or 9^{th} FREF harmonic for the "super" integer channel CKV=1872 MHz) would yield a sine wave of 8.5 kHz at baseband, which would be the rate of jitter induced on the FREF signal once passed through the AM to PM conversion within the victim circuit.

[0083] Simultaneously, the FREF 72^{nd} harmonic (for CKV=1872 MHz) would down convert the 68 kHz shift on CKV to a 68 kHz sine wave, and the 36^{th} harmonic of FREF would down convert the 34 kHz shift on the 936 MHz CKVD2 signal to a 34 kHz sine wave frequency-modulating FREF. Note that the 936 MHz interference can originate from the low-band divider once activated.

[0084] The relationship between the three low-frequency products in this example would not necessarily be that of the magnitude of the three high-frequency interferers from which they originated (i.e. CKV, CKVD2 and CKVD8), due to the nonlinear nature of the AM to PM operation, in which a stronger signal typically dominates.

[0085] A higher frequency product (i.e. 68 kHz in this example), may be a preferred one, as it is more effectively suppressed in the low-pass characteristics of the ADPLL relating its output phase to the FREF phase at its input.

The FREF Source

[0086] The FREF source, which is the victim of the interference in this model, is represented as a phase-modulation (PM) source, due to its conversion of additive interference, which may be represented as voltage/current, into phase-perturbations. A simple linear proportion factor α is assumed between the output phase and the input entity in this model, although a higher order dependency is also conceivable.

[0087] The transition intervals in the FREF signal, having short durations (e.g., 50-500 ps), may be regarded as sampling intervals, since only the interference induced during such intervals may impact the threshold crossing instance within it, thereby inducing a parasitic phase perturbation. At instances away from these transition intervals, the FREF signal would not be impacted by the interference signal, contrary to scenarios of linear addition. For this reason, in the model illustrated in FIG. **5**, the waveform at the output of the 26 MHz source is a train of impulses r(t) **135**, representing the sampling instances. These ideal impulses are input to a shaping filter **136**, whose time-limited impulse response p(t) corresponds to the duration of the rising edge in the FREF clock. The impulse response p(t) waveform represents the AM to PM conversion gain along that rising edge, which is naturally zero before the rising edge starts and after it is over, and may be high only during a very short interval around the threshold crossing in the rising edge (i.e. the pulse duration will not necessarily be equal in duration to the rise/fall time in FREF). The shaped pulses $r_p(t)$ **137** are then fed into a multiplier **138** where they sample the interference signal v(t) **149**.

[0088] Since only the rising edges (or falling edges) in FREF are used to drive the ADPLL logic, the train of impulses, representing the interference opportunities, have a period of T_s=1/26 MHz=38 ns, rather than 1/52 MHz (19 ns).

AM to PM Conversion (Creation of Jitter)

[0089] The signal b(t) **139** is responsible for the parasitic phase perturbations in the FREF signal, as shown in the interference model of FIG. **5**. Therefore, the low frequency content in b(t) will determine the amount of parasitic phase perturbations on the CKV signal at the output of the ADPLL, as it would survive the low-pass filtering of the ADPLL closed-loop transfer function.

[0090] The AM to PM conversion occurs as the additive interference b(t) creates a proportional phase-shift or zero-crossing time-shift (i.e. instantaneous jitter) within the DCXO slicer, and/or within the digital gates, around the instance the FREF signal crosses the threshold level within the victim circuitry, expressed as $\theta(t)=\alpha \cdot b(t)$ **141**.

Frequency Domain Representation and Creation of Low Frequency Interference

[0091] The train of impulses r(t) **135** in the time domain is equivalent, according to its well-known Fourier transform, to a train of Dirac functions in the frequency domain, separated by f_s=FREF=26 MHz in frequency (i.e. equal-power harmonics). The pulse shaping filter p(t) **136** may have a very narrow impulse duration (e.g., below 100 ps), which may be represented as a very wide low-pass filter in the frequency domain. A frequency-domain envelope representing this filter P(f) is to be applied, which could potentially have an effect around

the frequencies of interest. For example, for a width of 250 ps, corresponding to a bandwidth in the order of 1/250 ps=4 GHz, the second harmonic of CKV≈2 GHz, could be impacted. This is of interest, since it has been shown that the second harmonic of the transmitter's carrier frequency is dominant in this interference mechanism, rather than the derivatives of CKV.

[0092] For a pulse duration well below 100 ps, we may assume $R_p(f)=R(t)\cdot P(f)\cong R(f)$ for f<10 GHz. The expression in Equation 7 below provides the time-domain and frequency domain representations of the train of impulses corresponding to the sampling instances. The gain factor is not of interest, but it is important to note the rich harmonic content in R(f), which is counterintuitive given the spectrally clean FREF sinusoid.

$$r(t)=\sum_{n=-\infty}^{\infty}\delta(t-n\cdot T_S)\xrightarrow{Fourier}R(f)=\frac{2\pi}{T_S}\sum_{n=-\infty}^{\infty}\delta(f-n\cdot f_S) \tag{7}$$

$$R_p(f)=R(f)\cdot P(f)=\frac{2\pi}{T_S}\cdot P(f)\cdot\sum_{n=-\infty}^{\infty}\delta(f-n\cdot f_S) \tag{8}$$

where f=FREF=26 MHz.

[0093] The harmonic of FREF closest to the interfering signal (e.g., 2×CKV, CKV, CKVD2, CKVD8, DSP clock) serves to downconvert it to a near-zero frequency (or zero, for the integer-N channel case). This applies to the CKVD8 interference source when the integer ratio N is an integer multiple of eight, as is the case for the "super integer" channel CKV=1872 MHz, since then the CKVD8 clock frequency is at a harmonic of FREF.

[0094] The interference signal v(t) **149** in this case may be represented as follows.

$$v(t)=\sum_{k=1}^{L}A_k\cdot\mathrm{Cos}\{2\pi m_k f_S t+\varphi_k(t)\}\xrightarrow{Fourier}|V(f)|=\sum_{k=1}^{L}V_k(f)=\sum_{k=1}^{L}\tilde{A}_k\cdot C_k(f-m_k f_S) \tag{9}$$

[0095] $C_k(f)$ represents the magnitude-normalized spectrum of the modulated harmonic m_k. For example, those components in the summation in Equation 9 for which $m_k=2\times N$, represent the interference sources at the carrier's second harmonic at 2×CKV (e.g., those originating from the current surges in the TX and CKV dividers).

[0096] L represents the total number of interfering components located at harmonics of FREF represented by the integers $\{m_k\}$ (k=1, 2 . . . L). The sums in Equation 9 accommodate the possibility $m_j=m_k$ for j≠k, which would apply for independent sources of interference centered at the same FREF harmonic (e.g., from different circuits creating independent interference at a specific derivative or harmonic of CKV).

[0097] The frequency representation given in Equation 9 as a sum of spectra $V_k(f)$ illustrates that the total interference may be represented as L byproducts of the modulated carrier which are located at various harmonics of FREF having the appropriately compressed (for $m_k<N$) or expanded (for $m_k>N$) frequency deviations. It is noted that an expanded or compressed form of the modulated carrier's spectrum has a completely different appearance in the frequency domain, as it is the result of the Fourier transform of a frequency-modulated signal with a different modulation factor (i.e. not a GMSK signal for $m_k\neq N$).

[0098] As previously noted, for the values of the index k associated with the interfering components at the carrier frequency (i.e. at CKV), $m_k=N$, where $N=f_{carrier}/FREF$. In general, however, for some $1\leqq k\leqq L$, m_k may be greater than N. Based on laboratory observations, the dominant interferers of interest appear to be at the second harmonic of the carrier frequency, i.e. the M^{th} harmonic, where M=2×N. Furthermore, as previously noted, there may be two identical values for different elements in the vector m_k (i.e. $m_i=m_j$ for i≠j) since two different sources of interference at a specific harmonic may exist having independent amplitudes and phases (as is the case for the interfering signals from the separate TX and RX/CKV dividers).

[0099] In the expression of Equation 9, $\{A_k\}$ are the amplitudes of these modulated harmonics, and $\{\phi_k(t)\}$ are their time-variant phases. Despite the frequency synchronization between the interfering harmonics, they may arrive within the FREF circuitry at different phase shifts depending on the relative locations of the circuitry in which they are generated, and on their coupling mechanisms. Hence, the functions $\{\phi_k(t)\}$ satisfy the following relationships:

Synchronization of frequency modulation:

$$\frac{d}{dt}\varphi_n(t)=\frac{m_n}{N}f_{dev}(t) \tag{10}$$

Phase independence:

$$\varphi_n(t)=\Phi_n+2\pi\frac{m_n}{N}\int_{t_0}^{t}f_{dev}(t)dt=\Phi_n+\frac{m_n}{N}\cdot\varphi_c(t) \tag{11}$$

$$n=1,2\ \ldots\ L$$

where

[0100] $f_{dev}(t)$ is the frequency deviation experienced by the carrier as a result of the GMSK modulation of the transmitted data;

[0101] Φ_n is the initial phases for the n^{th} phase trajectory $\phi_n(t)$ at an arbitrary initial instance t_0, to which all the phase trajectory functions $\phi_n(t)$ are to be referenced;

[0102] $\phi_c(t)$ is the phase trajectory of the RF carrier whose time derivative is the carrier's instantaneous frequency deviation;

[0103] This frequency deviation signal $f_{dev}(t)$ follows the Gaussian filtering applied to the modulating data and reaches the nominal peak values of approximately $\Delta f_{peak}=\max\{f_{dev}(t)\}=\pm 68$ kHz.

[0104] Since there are interference contributors within v(t) that are of frequencies other than CKV (i.e. the carrier frequency during high-band operation), the multi-frequency sum v(t) contains elements of different frequency deviation magnitudes

$$\frac{m_n}{N}\cdot\Delta f_{peak}.$$

For the CKVD8 clock, for example, this relative magnitude is

$$\frac{m_n}{N}=\frac{1}{8}$$

(e.g., for 1872 MHz, N=72, and m=9). Consequently, the product of this component resulting from its down-conversions to zero by the m^{th} harmonic of FREF, has a different multiplying factor in its phase argument, thereby inhibiting its vector summation with the interfering components originating from the other modulated harmonics, centered at different frequencies, as explained in more detail infra.

[0105] The sampling operation, represented by multiplier **138** in the block diagram of FIG. **5**, performs the following multiplication:

$$b(t)=r_p(t)\times v(t)\xrightarrow{Fourier} \tag{12}$$

$$B(f)=R_p(f)*V(f) \tag{13}$$
$$=\left[\frac{2\pi}{T_S}\cdot P(f)\cdot\sum_{n=-\infty}^{\infty}\delta(f-n\cdot f_S)\right]*\sum_{k=1}^{L}\tilde{A}_k\cdot C_k(f-m_k f_S)$$

[0106] The products of interest in the above frequency domain convolution are those resulting from the relocation of the spectra $C_k(f-m_k\cdot f_s)$ to zero, as for each m_k there is a Dirac function in $R_p(f)$ satisfying $n=m_k$.

[0107] Specifically, for those values of k where $m_k=M$, the interfering signals at the second harmonic of the carrier frequency (e.g., from the current surges feeding the TX divider and from those of the CKV circuitry driven by the RX/CKV divider) will be down converted to zero by the M^{th} harmonic of FREF within $R_p(f)$. The result of interest within B(f), which is around f=0, may be represented as the sum:

$$\left|\tilde{B}(f)\right|=\sum_{i=1}^{K}\tilde{A}_i\cdot|C_i(f)| \tag{14}$$

where

[0108] K<L represents the actual number of the interfering components of interest (at the second harmonic of the carrier frequency in this case);

[0109] $C_i(f)$ are the spectra for these interfering signals after their down conversion to zero;

[0110] In the time domain, the zero-centered interference product b(t) may be expressed as the sum of the time domain zero-IF down-converted signals as follows.

$$b(t)=\sum_{i=1}^{K}\tilde{A}_i\cdot\mathrm{Cos}\{\varphi_i(t)+\Phi_i\} \tag{15}$$

[0111] Since the $\phi_i(t)$ phase trajectories considered here are only those originating from the interferers at the second harmonic of the carrier frequency, for all values of the index i, $\phi_i(t)$ may be replaced with $2\times\phi_c(t)$, further simplifying the sum to the form:

$$b(t)=\sum_{i=1}^{M}\tilde{A}_i\cdot\mathrm{Cos}\{2\varphi_c(t)+\Phi_i\}=A_{total}\cdot\mathrm{Cos}\left\{\int_0^t\omega_0(\tau)d\tau+\Phi_0\right\} \tag{16}$$

[0112] This type of trigonometric summation may be represented as a vector sum. In this case, all elements are phasors centered at f=0, having different amplitudes A_i and different phases Φ_i. It is noted that:

$$\omega_o(t)=\frac{d}{dt}2\varphi_c(t)\neq\text{constant, mean}\{\omega_o(t)\}=0 \tag{17}$$

[0113] Therefore, the phasors in Equation 16 are not of constant frequency, but since they share the same time-varying phase $2\phi_c(t)$, or equivalently, the same instantaneous frequency, they may be summed in vector form.

[0114] Contrarily, a down-converted product of CKVD8, having a time varying phase of

$$\frac{1}{8}\varphi_c(t),$$

cannot be considered in this manner and added to this sum in vector form, since its instantaneous frequency deviation is divided by a factor of 8 in the divide-by-8 operation.

[0115] The sum of all K elements having identical instantaneous frequency is represented in Equation 16 as a single trigonometric function at a zero-IF frequency of instantaneous value $\omega_0(t)$ having the magnitude A_{total} and the phase shift Φ_0.

Impact of the Phase Shift Φ_0 on the Interference Effect

[0116] Interestingly, the phase shift Φ_0 in the expression for the interference signal b(t) in Equation 16 is of great importance, as it determines the impact of the interfering signal. Although it represents a fixed relative phase between the interference signal b(t) and the FREF victim, to which the interfering harmonics are frequency synchronized, it could determine the spectral content of b(t) due to the nonlinear trigonometric function in which it appears in Equation 16. A specific known case in which it would not have an effect on the spectral content, is for $\omega_0(t)=\beta$, where β is a constant representing a fixed phase-slope. For this case, the expression in Equation 16 has the form of a tone centered at $\omega=\beta$[rad/sec] as express below.

$$b(t)=A_{total}\cdot\mathrm{Cos}\{\beta\cdot t+\Phi_0\} \tag{18}$$

[0117] For this case, the spectrum |B(f)| of the interfering signal will not be affected by the phase shift Φ_0 as it is simply a Dirac function at $\omega=\beta$ in the frequency domain. The expression in Equation 18 would apply in the interference scenario whenever redundant data is transmitted, such as only '1's or only '0's, both of which result in a fixed frequency shift from

the carrier. In such cases, the down converted interference results in a tone at double the 67.7 kHz frequency shift, i.e. $\beta=2\cdot\pi\cdot135.4=850.85$ k rad/sec.

[0118] The AM-to-PM conversion of this interfering tone within the FREF circuitry results in frequency modulation at the rate of 135.4 kHz, creating spurs at frequency distances that are integer multiples of this frequency around FREF. The level of these spurs, corresponding to the extent of interference, are unaffected by the phase shift Φ_0 and hence such redundant modulation is not useful for the observation and investigation of the TX performance dependency upon the FREF-RF phase relationship.

[0119] It is further noted that as the FREF source undergoes the parasitic phase modulation described above, the down converting harmonic of it at 2×CKV or M×FREF may no longer be assumed to be a simple Dirac function. This is also the case for modulation with random data, for which the phase perturbations induced onto FREF would not be represented by a simple tone. This compound effect is neglected, however, in the analysis as it is weak compared to the intentional modulation present on the carrier and its harmonics. This signal-to-noise assumption becomes even more valid once the phase alignment Φ_0 is properly tuned, thus minimizing the interference and maximizing the ratio between the desired and parasitic phase modulations on the carrier to achieve the optimal phase-error performance.

Vector Summation of the Interference Sources

[0120] A vector diagram for multiple interference sources at the second harmonic is shown in FIG. **6**. This figure graphically illustrates the vector sum of expression Equation 15, where only two interference sources are assumed to be present, both of which share the same instantaneous frequency. The RX or CKV divider has four different orthogonal phases indicated as: vector **160** at basic phase 0 degrees, vector **162** rotated −90 degrees, vector **164** rotated 180 degrees and vector **166** rotated 90 degrees. Each vector of which may be selected to drive the TDC and the CKV based digital circuitry. Laboratory observations confirm that the magnitude of interference suffered at FREF, resulting in different levels of RMS PHE, is linked with this phase selection.

[0121] The vector diagram in FIG. **6** illustrates how a specific phase relationship between the interferences from the RX and the TX dividers, which is dictated by the values of the phase "biases" Φ_i, can yield four different magnitudes for the total interference, depending on the selected phase for the RX divider. For each selected phase, the vector sum (vector **168**) is not only different in magnitude but also in its phase relationship with FREF, which has been shown to affect the extent of degradation in RMS phase error (PHE) performance. The phase between the vector sum **168** and FREF, however, could be adjusted via software, allowing the minimization of the impact of this interference.

[0122] In FIG. **6**, the vector sum having magnitude A_{total} and phase Φ_0, is shown for the case where the selected RX divider phase is 0. The lowest level of interference, and hence the preferable one, is clearly observed for the case where the −90 degree phase output of the RX divider is selected instead.

Spectral Analysis of the Parasitic Phase Perturbations θ(t)

[0123] It should be noted that due to the nonlinear nature of the trigonometric Cos function, the spectral content of b(t) may be very different from that of its phase argument function γ(t) expressed in Equation 19 below. As has been previously stressed, even the constant phase bias Φ_0 within this function has an effect on the spectral content of b(t) and can shift spectral content around in the frequency axis while not affecting the total power in the signal b(t). This is in contrast to its effect within γ(t) itself, where only the DC level is affected while all other frequency content in γ(t) remains unaffected.

[0124] The phase relationships Φ_i of the multiple interferers (with respect to each other and FREF) determine the magnitude A_{total} of the total interference b(t), as well as its phase Φ_0. Both the magnitude and the phase of the interference impact transmitter performance. The amount of interference suffered is proportional to the magnitude of b(t), but is also dependent on its phase, since the spectral content is dependent on this phase, as previously explained, and when the spectrum of the interference is concentrated more within the loop bandwidth of the ADPLL, its potential impact is greater.

$$b(t)=A_{total}\cdot\mathrm{Cos}\{2\phi_c(t)+\Phi_0\}=A_{total}\cdot\mathrm{Cos}\{\gamma(t)\} \quad (19)$$

[0125] A graph illustrating the periodic characterization of the phase dependency is shown in FIG. **7**. Trace **172** represents the mean RMS phase error for 100 GSM bursts, while trace **170** represents the maximum RMS phase error for 100 GSM bursts. A graph illustrating the theoretical RMS and peak of interference and proportional jitter versus RF/FREF phase shift is shown in FIG. **8**.

Interference Minimization Mechanisms

[0126] Presented below is a description of how a properly selected phase shift Φ_0 serves to minimize the impact of the interference by substantially pushing its spectral content outside of the ADPLL loop bandwidth. Additionally, the use of intentional phase-perturbations induced onto FREF, serving for the same purpose, will be described. The latter remedy to the interference problem is referred to as the hardware based dithering solution to the phase error problem as described in detail herein. The former remedy is based on phase alignment of the interference and is implemented as a software fix solution.

DCXO FREF Phase Dithering

[0127] The spectrum R(f) of the hypothetical sampling signal r(t) in Equation 7 has been shown to be a series of Dirac functions centered at harmonics of the FREF frequency. This representation holds valid as long as the FREF signal carries no modulation, as is typically the case for a reference signal of a PLL. Once the FREF signal is purposefully frequency modulated with a phase-dithering signal, however, the sidebands of the resultant frequency modulation on the higher harmonic of it would be stronger by a factor of M (i.e. the ratio between the frequency of harmonic at M×FREF or 2×CKV, and the fundamental 26 MHz). Equivalently, the frequency deviation experienced by the M^{th} harmonic of FREF is M times wider. For example, consider the integer channel 1872 MHz, where N=72 and M=144, a frequency deviation of 100 Hz on FREF translates to 14.4 kHz of deviation at a second harmonic of 1872 MHz. This 'amplified' deviation is down converted to zero, where it is added onto the phase modulation existing on the second harmonic of the RF signal at 2×CKV.

[0128] For example, if the frequency-dithering signal being applied is a 2 MHz square wave of 100 Hz magnitude, then the

phase dithering signal is a triangular wave amplified by a factor of M, which is summed with the phase modulation signal $2\times\phi_c(t)$ as it is being down-converted to zero.

[0129] In accordance with the invention, since the interfering signal can be represented by the nonlinear trigonometric transfer function given above, the addition of the dithering signal results in intermodulations that effectively push a great portion of the interference energy outside of the frequency band of interest.

First Example Embodiment

[0130] A diagram illustrating an example single chip radio incorporating a first embodiment of the frequency reference dithering mechanism of the present invention is shown in FIG. **9**. The single chip radio IC, generally referenced **200**, comprises a silicon die **204** having a plurality of bond pads **211** connected via bond wires **212** to pins, balls, etc. **213** depending on the type of IC packaging used. The die **204** comprises a plurality of etched circuits including the FREF slicer **208**, DCXO circuit **202**, ADPLL **210**, TX RF circuit **215** and dither signal generator circuit **206** of the present invention. Note that there could be two types of dithering: single or multiple clock sources.

[0131] In operation, the output of the crystal **217** is routed to the DCXO **202** and to the slicer circuit via a bond wire **203**. In accordance with the present invention, a dither signal is generated and routed to a bond wire **205** in close physical proximity to the bond wire **203** carrying the frequency reference signal from the crystal. Coupling of the dither signal (indicated by dotted arrow **207**) to the frequency reference signal significantly reduces the effects of the interference caused by coupling of the transmit RF signal (or internal digital RF signal) back to the frequency reference input. It is noted that in highly integrated RF transceivers or single-chip radios, the spatial separation between the aggressor(s) and victim(s) is very difficult to achieve.

[0132] The frequency beating of the FREF signal by the dither signal causes the FREF clock signal to go in and out of integer multiples of the transmit RF output signal in a random manner. The dithering of the FREF randomizes and moves the zero crossings of the frequency reference source such that when the TX RF output coupling aligns at what used to be an integer multiple in frequency, the alignment does not happen in the same spot. The randomization effectively reduces by 90-95% the occurrences of the alignment whereby the TX RF output frequency is an integer multiple of the frequency reference.

Second Example Embodiment

[0133] A diagram illustrating an example single chip radio incorporating a second embodiment of the frequency reference dithering mechanism of the present invention is shown in FIG. **10**. The single chip radio IC, generally referenced **220**, comprises a silicon die **222** having a plurality of bond pads **223** connected via bond wires **225** to pins, balls, etc. **227** depending on the type of IC packaging used. The IC die **222** comprises a plurality of etched circuits including the DCXO **224**, FREF slicer **226**, ADPLL **228**, TX RF circuit **238** and dither signal generator circuit **230** of the present invention.

[0134] In this embodiment, controlled direct coupling is introduced into the circuit in order to realize direct coupling of the dither signal to the frequency reference input. This direct coupling technique can be useful when the indirect coupling technique described supra is not practical. The controllable coupling may comprise magnetic coupling, electrical resistive coupling or capacitive coupling or any combination thereof. In the example embodiment presented herein, capacitance coupling is used.

[0135] In operation, the output of the crystal **239**, is routed to the slicer **226** and DCXO **224** via series capacitor **221** bond wire **237**. In accordance with the present invention, a dither signal is generated and routed to a bond wire **233**. An external coupling circuit **234** couples the dither signal either directly to the bond wire **237** carrying the frequency reference signal output of the crystal **239**. The coupling may comprise any suitable coupling circuit and in the example embodiment presented herein comprises an RC circuit including capacitor **232** and resisters **236**, **229** that form a voltage divider. The dither signal is thus coupled to the reference frequency input via capacitive coupling through an external coupling circuit. Direct coupling of the dither signal to the frequency reference signal significantly reduces the effects of the interference caused by coupling of the transmit RF signal back to the frequency reference input in the same manner as described above.

[0136] In addition, the level of dithering can be 'tuned' by adjusting either up or down the value of the coupling capacitor from a nominal value of 0.5 pF. Further, the resistive divider network comprising resisters **229**, **236** can optionally be used to control the magnitude of the dithering signal. Note also that the frequency reference circuit can be dithered using any clock signal by varying the threshold voltage in the associated slicer circuit. This de-sensitizes the RF signal conversion into frequency timestamp deviations by applying a strong but periodical stimulus.

[0137] Note that the test circuit **236** is shown only for example purposes to illustrate the connection of the dither signal to an unused pin of the chip. In this example, the test circuit is used during manufacturing test procedures and is not in use during normal operation of the chip. It is important, however, that the dither signal be applied to a pin whose bond wire is close enough to that of the frequency reference to mitigate the interference.

[0138] Thus, the principle of the present invention, is that the interfering RF signal is sampled by the FREF slicer, such that it effectively is downconverted to zero-IF. There, at low frequencies, it is translated in the slicing operating into low-rate jitter that passes through the low-pass characteristics of the low pass transfer function of the ADPLL (i.e. from FREF phase to RF phase). By adding an additional high-frequency signal before the slicer, and thus dominating the jitter on it and bringing it into higher frequencies where the low-pass response of the ADPLL is able to suppress it, the noticeable impact on the RF jitter (i.e. phase distortions) is significantly reduced. In particular, it is the frequency translation and/or compression characteristic of the non-linear voltage domain transfer function response of the slicer that is responsible for the desensitization of the ADPLL to the RF interfering signal.

Dither Signal Generator

[0139] A block diagram illustrating the dither signal generator of the present invention in more detail is shown in FIG. **11**. The dither signal generator, generally referenced **240**, comprises a slicer or other optional clock conditioning circuit **242**, clock divider circuit **244** and multiplexer **246**.

[0140] In operation, the FREF signal **250** from the DCXO is input to the slicer **242** which outputs a square wave clock

signal CK**26** **252** at 26 MHz (assuming 26 MHz frequency reference signal input). The CK**26**, CKV, or any other clock is input to a counter which functions to divide the clock into a plurality of slower clock signals. In this example, clocks at 2, 4, 8 and 16 MHz are generated. The clock divider may also divide the available clock (i.e. FREF) by power or two (i.e. 13 MHz, 6.5 MHz, etc.). The output dither signal **254** is generated by switching between two or more of the clock signals output from the clock divider, e.g., the 0.8 and 1.6 MHz signals. It is appreciated that dither signals comprising other combinations of two or more clock signals may be used as well depending on the particular implementation.

[0141] The clock signal that is to be output as the dither signal is selected via the mux control signal **248** supplied by a control circuit such as the script processor **274** (FIG. **2**A). At any one time, only a single clock signal is selected by the multiplexer **246**. The action of switching between two or more clock signals generates a dither signal that, when coupled to the reference frequency input, is able to apply sufficient randomness to the zero crossings of the reference for double dithering frequency input to mitigate the interference effect of the transmit RF output signal. The double dithering also improves the far out noise performance.

[0142] Although the dither signal in this embodiment has been constructed from the frequency reference clock (FREF) which already exists internally in the radio, it is appreciated that any suitable dither generating circuit can be used. For example, a dedicated pseudo-noise sequence generator can be as well to generate the dither signal. In fact, any source, either dedicated or re-used from some existing signals and circuits, can be used to overcome the interference on FREF.

RMS Phase Error Improvement

[0143] As described supra, the RMS phase error of the ADPLL is reduced by use of the frequency reference dithering mechanism of the present invention. To illustrate the improvement possible with the present invention, phase error measurements for an ADPLL based transmitter circuit is presented below in Table 1. Data for the two cases of an ADPLL circuit with and without the frequency reference dithering mechanism of the present invention is provided.

TABLE 1

Max RMS phase error for selected frequencies

	MAX RMS Phase Error					
	−40° C.		25° C.		80° C.	
RF Frequency	Dither ON	Dither OFF	Dither ON	Dither OFF	Dither ON	Dither OFF
1716 MHz	2.63	3.28	2.7	4.03	2.87	4.1
1742 MHz	2.55	3.3	2.85	3.85	3.02	4.17
1872 MHz	2.6	3.65	2.85	4.29	2.8	4.36

[0144] Considering a requirement of 3 degrees of RMS permitted phase error, the circuit without the dithering mechanism does not meet the specification.

[0145] Further illustration of the improvement of the phase error in a cellular phone environment with the dithering mechanism is provided below in Table 2 which presents measurements of maximum phase error with and without dithering for selected GSM channels.

TABLE 2

Max RMS phase error for selected GSM channels

Channel No.	Max PHE without dither (degrees)	Max PHE with dither (degrees)
CH541	5.6	3.2
CH606	3	2.5
CH671	5.4	2.5
CH736	3.5	2.5
CH801	5.3	3
CH866	3.1	2.6

[0146] The max PHE is significantly improved when dithering is used. All the channels with the exception of CH541 meet the specification of 3 or less degrees of RMS phase error.

[0147] It is intended that the appended claims cover all such features and advantages of the invention that fall within the spirit and scope of the present invention. As numerous modifications and changes will readily occur to those skilled in the art, it is intended that the invention not be limited to the limited number of embodiments described herein. Accordingly, it will be appreciated that all suitable variations, modifications and equivalents may be resorted to, falling within the spirit and scope of the present invention.

1. A method of minimizing the impact of interference to a frequency reference input from a radio frequency (RF) signal, said method comprising the steps of:

generating a dithering signal; and

coupling said dithering signal to said frequency reference input to generate a modulated frequency reference signal modulated with said dithering signal.

2. The method according to claim **1**, wherein said step of generating comprises generating a phase dithering signal.

3. The method according to claim **1**, wherein said step of generating said dithering signal comprises switching between a plurality of clock signals of different frequencies.

4. The method according to claim **1**, wherein said step of coupling comprises applying said dithering signal to a first bond wire located in close physical proximity to a second bond wire corresponding to said frequency reference input.

5. The method according to claim **1**, wherein said step of coupling results in intermodulations that effectively shift a significant portion of interference energy outside a particular band of interest.

6. The method according to claim **1**, wherein said step of coupling comprises coupling said dithering signal via an external coupling circuit to a first bond wire located in close physical proximity to a second bond wire corresponding to said frequency reference input.

7. The method according to claim **1**, wherein said step of coupling comprises directly coupling said dithering signal to said frequency reference input via an external coupling circuit.

8. The method according to claim **7**, further comprising a resistive divider network in series with said external coupling circuit, said resistive divider network operative to control the magnitude of said dithering signal.

9. The method according to claim **1**, wherein said step of coupling said dithering signal effectively moves the zero

crossings of said frequency reference signal such that the frequency at which said transmit RF signal is an integer multiple of said reference frequency is randomized.

10. The method according to claim **1**, wherein the frequency of said RF signal is an integer-N multiple of said frequency reference input.

11-45. (canceled)

46. The method according to claim **1**, wherein said dithering signal is periodic.

47. The method according to claim **4**, wherein said dithering signal is periodic.

48. The method according to claim **5**, wherein the dithering signal is periodic.

49. The method according to claim **6**, wherein said dithering signal is periodic.

* * * * *