An embodiment of the present invention provides transmitter having a phase locked loop that has a dynamically controllable loop bandwidth. A transmit modulator is coupled to the PLL for performing vector modulation in response to transmission symbols. Each transmission symbol comprises an amplitude signal and a phase signal. A controller is coupled to the PLL and to the transmit modulator and is operable to detect when a criteria of the transmission symbols crosses a threshold and to adjust loop bandwidth in response to crossing the threshold. The criteria of the transmission symbols may be a function of the amplitude signal or a function of the phase signal, and may be the amplitude signal, a first derivative of the amplitude signal, a second derivative of the amplitude signal, a square of the amplitude signal, a derivative of the amplitude signal squared, the phase signal, or a derivative of the phase signal.
Note:
States S3 and S5 are bypassed in Simple Mode.

IDLE and S4: HW_GEARSHIFT_WIDE = 0, TIMER_START = 0
S1 and S3: HW_GEARSHIFT_WIDE = 1, TIMER_START = 1
S2 and S5: HW_GEARSHIFT_WIDE = 1, TIMER_START = 0
TRANSMITTER PLL WITH BANDWIDTH ON DEMAND

CLAIM OF PRIORITY UNDER 35 U.S.C. 119(c)

[0001] The present application claims priority to and incorporates by reference U.S. Provisional Application No. 61/076,801 filed Jun. 30, 2008, entitled “Transmitter PLL with Bandwidth on Demand”.

FIELD OF THE INVENTION

[0002] This invention generally relates to the field of control systems and data communications. In particular, it relates to cellular telephony and communication devices such as Bluetooth, WLAN, etc. using digital radio frequency (RF) circuitry.

BACKGROUND OF THE INVENTION

[0003] Wireless cellular communication networks incorporate large numbers of mobile user equipment (UEs) and a number of base nodes (NodeBs). A NodeB is generally a fixed station, and may also be called a cell transceiver system (BTS), an access point (AP), a base station (BS), or some other equivalent terminology. As improvements of networks are made, the NodeB functionality evolves, so a NodeB is sometimes also referred to as an evolved NodeB (eNB). In general, NodeB hardware, when deployed, is fixed and stationary, while the UE hardware is typically portable.

[0004] In contrast to NodeB, the mobile UE can comprise portable hardware. User equipment (UE), also commonly referred to as a terminal or a mobile station, may be fixed or mobile device and may be a wireless device, a cellular phone, a personal digital assistant (PDA), a wireless modem card, and so on. Uplink communication (UL) refers to a communication from the mobile UE to the NodeB, whereas downlink (DL) refers to communication from the NodeB to the mobile UE. Each NodeB contains radio frequency transmitter(s) and the receiver(s) used to communicate directly with the mobiles, which move freely around it. Similarly, each mobile UE contains radio frequency transmitter(s) and the receiver(s) used to communicate directly with the NodeB. Cellular networks, the mobiles cannot communicate directly with each other but have to communicate with the NodeB.

[0005] With each successive cellular phone handset generation, users demand more features in a smaller form factor. Some recent examples include cell phones with integrated Bluetooth, GPS, digital camera, and MP3 functionality. Process shrinks help deliver a cost and size advantage for digital designs with relative ease. However, for analog/RF designs, the immaturity of advanced processes comes with design challenges that may outweigh the intended advantage. In a older generation handsets, 30 to 40% of handset board space is occupied by analog/RF functionality which cannot be redesigned or migrated to the newer process/technology nodes easily, inhibiting vendor ability to cost effectively add features and reduce footprint.

[0006] Digital radio has recently allowed the replacement of space consuming analog RF circuitry with much more compact digital circuitry, thereby facilitating the ability to port designs rapidly to more advanced lithographies. Texas Instruments (TI) has proven this concept with its Digital RF Processor (DRP™) architecture, which it has successfully implemented in production versions of its Bluetooth BRF6xxx transceivers, GSM/GPRS LoCosto TCS23xx transceivers among other chips. DRP implementation is consistent with the on-going trend toward RF-CMOS in the cellular area, making it attractive in terms of power consumption, cost, and the integration of multiple radios.

[0007] Oscillators are a key component in the design of radio frequency (RF) communication systems. The estimation and calibration of the modulation gain of an RF oscillator is currently an area of active research. Accurate knowledge of this gain significantly reduces the complexity and increases the performance of the phase-locked loop (PLL) as well as the transmit frequency modulation path. It is particularly beneficial in systems implemented in deep submicron and nanoscale CMOS and based on orthogonal frequency/amplitude (i.e. polar) topology. Estimation of RF oscillator frequency-modulation gain is especially important in low-cost dominantly digital high-volume transceivers. In such systems, the phase locked loop sets the loop bandwidth while the transmitter sets the transfer function of the direct frequency modulation path wherein the acceptable gain estimation error ranges from less than 1% for LTE/WCDMA to several percent for EDGE (Enhanced Data rates for GSM Evolution), GSM and Bluetooth, for example.

[0008] An all-digital frequency synthesizer architecture built around a digitally controlled oscillator (DCO) that is tuned in response to a digital tuning word (OTW) is described in U.S. Pat. No. 7,046,098 entitled “All-digital frequency synthesis with capacitive re-introduction of dithered tuning information” and is incorporated by reference in its entirety herein.

[0009] All known EDGE transmitters are affected by modulation distortion due to the RF oscillator pulling by the transmitted RF output and supply-ground coupling of extraneous noise sources. Whether using a polar or I/Q TX modulator, the instantaneous transmitted frequency at the SoC (system on a chip) output or PA (power amp) output is different from the resonant frequency of the RF oscillator, thus creating a frequency pulling force. Correspondingly, supply-ground coupling of extraneous noise and current spikes generated by other circuits on the same die causes frequency pulling of the oscillator.

[0010] In a typical EDGE transmitter, amplitude modulation of the pre-power amplifier (PPA) causes frequency pulling of the DCO thus leading to the degradation in error vector magnitude (EVM). The pulling problem is currently solved in industry by (1) significantly increasing the loop bandwidth; (2) using offset PLL architecture that is based on non-harmonic frequency planning. Both of these methods significantly increase the hardware complexity and consumed power.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Particular embodiments in accordance with the invention will now be described, by way of example only, and with reference to the accompanying drawings:

[0012] FIG. 1 is a pictorial of an illustrative telecommunications network that employs an embodiment of bandwidth on demand in transceivers used in the network;

[0013] FIG. 2 is a block diagram of a single-chip radio with an all-digital local oscillator and transmitter and a discrete-time receiver;

[0014] FIG. 3 is a more detailed block diagram illustrating the all-digital phase locked loop (ADPLL) based polar transmitter of FIG. 1 constructed in accordance with the present invention;
A key component of transmitter is a digitally controlled oscillator (DCO) that is part of an interpolated all-digital phase-locked loop (ADPLL). The DCO avoids any analog tuning controls. The DCO generates a high-quality base station-synchronized frequency reference such that the transmitted carrier frequencies and the received symbol rates are accurate to within 0.1 ppm.

In the current embodiment of the ADPLL architecture, which is strictly optimized for low area and power consumption, maintaining an excessive ADPLL bandwidth all the time in order to manage noise induced oscillator pulling would degrade spectral mask by less filtering of the reference and TDC (time to digital converter) phase noise. Embodiments of the present invention dynamically increase the ADPLL loop bandwidth only when it is really needed. During the course of modulation, the significant pulling force exists only for a fraction of the time. Therefore most of the time it is not strong enough to create a noticeable degradation in error vector magnitude (EVM). Engaging a wide ADPLL bandwidth only at the time of strong frequency pulling mitigates its negative effects and leads to only a small increase in the close-in phase noise. For example, if the duty cycle of the wide bandwidth is 50% then the resultant modulation spectrum will be midway between that of the normal bandwidth and wide bandwidth. Typically, the wide bandwidth duty cycle will be much less than 50%.

An advanced All-Digital PLL (ADPLL) frequency synthesizer is described in US Patent application 2008-0315960 to Waheed et al entitled “Digital Phase Locked Loop with Gear shifting” which is incorporated by reference herein in its entirety. Portions of the ADPLL that are relevant to embodiments of the present invention are also described herein. This advanced all-digital frequency synthesizer possesses two-point digital, i.e., reference and direct, frequency modulation capability. ADPLL uses digital signal processing and efficient circuit design techniques. A 4 or 8 GHz digitally-controlled oscillator (DCO) is at the heart of ADPLL, where fine frequency resolution is achieved through high-speed sigma-delta (ΣΔ) dithering. This setup allows for ADPLL loop control circuitry to be implemented in a fully digital manner using Infinite Impulse Response (IIR) filters and a digital Proportional-integral (PI) controller. For the feedback of DCO phase in the time-domain, very fine time resolution (~20 ps) is achieved by employing a Time-to-Digital Converter (TDC) comprising a chain of digital inverters.

The ADPLL architecture is distinct in that the loop filter and bulk of the logic operates on an RF derived variable clock domain. Due to the common RF based clock source for the major digital components, convenient digital handoff is achieved in the signal paths. The architecture uses two resamplers (one linear and the other a simple zero-order hold) for the exchange of data from and to the reference clock domain to the variable RF clock domain. In the variable clock domain, availability of several edge-aligned clock domains also facilitate physical register transfer logic (RTL) hardware sharing by time slicing. ADPLL can be embodied by more than one arrangement of the resampler and the other digital blocks. While several embodiments will be described herein, these descriptions are not intended to be limiting.

A key component of transmitter is a digitally controlled oscillator (DCO) that is part of an interpolated all-digital phase-locked loop (ADPLL). The DCO avoids any analog tuning controls. The DCO generates a high-quality base station-synchronized frequency reference such that the transmitted carrier frequencies and the received symbol rates are accurate to within 0.1 ppm.
The radio circuit, generally referenced 130, comprises a radio integrated circuit 136 coupled to a crystal 152, antenna front end module 176 connected to antenna 180 and battery management circuit 132. The radio chip 136 comprises a script processor 146, digital baseband (DBB) processor 144, memory 142 (e.g., static RAM), transmit (TX) block 148, receiver (RX) block 150, digitally controlled crystal oscillator (DCXO) 154, slicer 156, power management unit 138, RF built-in self test (BIST) 140. Battery 134 and battery management circuit 132 are connected to radio chip 136 for providing power. The TX block comprises high speed and low speed digital logic block 158 including sigma-delta (ΣΔ) modulators 160, 162, digitally controlled oscillator (DCO) 164, digitally controlled power amplifier (DPA) 174 or pre power amplifier (PPA), time-to-digital converter (TDC) circuit 170 and TDC quantization noise shaping block 166. The transmitter generates various radio frequency signals, as defined by the 3GPP specifications. For example, the transmitter may support one or more of the 3G UMTS frequencies: 850, 900, 1700, 1900, or 2100 MHz.

A key component of transmitter block 148 is digitally controlled oscillator (DCO) 164, that is part of an interpolated-digital phase-locked loop (ADPLL). DCO 164 avoids any analog tuning controls. The DCO generates a high-quality base station-synchronized frequency reference such that the transmitted carrier frequencies and the received symbol rates are accurate to within 0.1 ppm. Fine frequency resolution is achieved through high-speed sigma-delta (ΣΔ) dithering of its varactors. Digital logic built around the DCO realizes an interpolated all-digital PLL (ADPLL) that is used as a local oscillator for both the transmitter and receiver. The polar transmitter architecture utilizes the wideband direct frequency modulation capability of the ADPLL and a digitally controlled power amplifier (DPA) 174 for the amplitude modulation. The DPA operates in near-class-Ⅱ mode and uses an array of nMOS transistor switches to regulate the RF amplification and acts as a digital-to-RF amplitude converter (DRAC). It is followed by a matching network and an external antenna front-end module 176, which comprises a power amplifier (PA), a transmit/receive switch for the common antenna 180 and RX surface acoustic wave (SAW) filters. Fine amplitude resolution is achieved through high-speed ΣΔ dithering of the DPA nMOS transistors. The ADPLL also comprises TDC quantization noise shaping block 166 operative to reduce the quantization noise contribution of the TDC. It is noted that the TDC quantization noise shaping mechanism is especially applicable in the ADPLL circuit.

The receiver employs a discrete-time architecture in which the RF signal is directly sampled and processed using analog and digital signal processing techniques. RX block 150 comprises a low noise transconductance amplifier 182, current sampler 184, discrete time processing block 186, analog to digital converter (ADC) 188 and digital logic block 190. The receiver 150 employs a discrete-time architecture in which the RF signal is directly sampled at the Nyquist rate of the RF carrier and processed using analog and digital signal processing techniques. The receiver is integrated with a script processor 146, dedicated digital base band processor 144 (i.e. ARM family processor and DSP) and SRAM memory 142. The script processor handles various TX and RX calibration, compensation, sequencing and lower-rate data path tasks and encapsulates the transceiver complexity in order to present a much simpler software programming model.
implements various DPA calibration and BIST procedures. The transceiver is integrated with the digital baseband, SRAM memory in a complete system-on-chip (SoC) solution.

[0041] Almost all the clocks on this SoC are derived from and are synchronous to the RF oscillator clock. This helps to reduce susceptibility to the noise generated through clocking of the massive digital logic. A fixed clock module (not shown) provides a buffered fixed clock signal that provides timing for DBB 144, script processor 146, SRAM 142 and other functional logic. In this embodiment, the fixed clock is derived from the variable RF oscillator clock CKVx. In other embodiments, the fixed clock could be derived from the reference clock produced by DCXO 154, or from another independent clock source.

[0042] FIG. 3 is a more detailed block diagram of an ADPLL 200 used in the transceiver of FIG. 1 and constructed in accordance with the present invention. For illustration purposes only, the transmitter of the present embodiment is adapted for the GSM/EDGE cellular standard. It is appreciated, however, that one skilled in the communication arts can adapt the transmitter illustrated herein to other modulations and communication standards as well without departing from the spirit and scope of the present invention. For example, the transmitter illustrated in FIG. 3 can be extended for performing an arbitrary quadrature modulation scheme.

[0043] A description of the ADPLL, generally referenced 200, including the frequency/phase modulation path is provided herein below. The core of the ADPLL is a digitally controlled oscillator (DCO) 228 adapted to generate the RF oscillator clock CKV. The oscillator core (not shown) operates at twice the 1.6-2.0 GHz high frequency band or four times the 0.8-1.0 GHz low frequency band. The output of the DCO is then divided for precise generation of RX quadrature signals, and for use as the transmitter’s carrier frequency. For GSM/EDGE transceivers, a single DCO is shared between transmitter and receiver and is used for both the high frequency bands (HB) and the low frequency bands (LB). However, for modern 3G (WCDMA) or other duplex transmission systems, separate local oscillators might be needed to supply TX and RX carrier frequencies.

[0044] A digitally-controlled oscillator (DCO) lies at the heart of the interpolated all-digital PLL (ADPLL) frequency synthesizer. It deliberately avoids any analog tuning voltage controls and is realized as an ASIC cell with truly digital inputs and outputs. The DCO comprises tunable switchable varactor elements, cross-coupled pairs of NMOS transistors, and a biasing circuit. The DCO varactors may be realized as n-poly/n-well MOS capacitor (MOSCAP) devices that operate in the flat regions of their C-V curves. Current advanced CMOS process lithography allows creation of extremely small-size but well-controlled varactors. The switchable capacitance of the finest differential TB varactor is in tens of attofarads. This resolution, however, is still too coarse for wireless applications and requires high-speed 2A differencing to enhance the time-averaged frequency resolution. The output of the DCO is input to the RF high band power amplifier 234. It is also input to the RF low band power amplifier 232 after divide by two in divider 230.

[0045] In case of transmit modulation, the symbols, (for example GSM, EDGE, WCDMA, etc.), in the form of in-phase and quadrature data streams are received from the digital baseband (DBB) circuit 144 in FIG. 2 and the GSM symbols are passed through a pulse-shaping filter (PSF) within processor 212 that converts it to phase modulation. This phase modulation is interpolated in transmit data (DTX) processing circuit 250 and then passed on to the ADPLL after differentiation at the CKVD16 clock rate using differentiator 252. CKV is the ADPLL RF output digital variable clock in case of high-bands (HB> 1 GHz) or twice the RF output clock in case of low-band (LB, <1 GHz).

[0046] For the case of EDGE, WCDMA, etc., the complex vector modulation I/Q (in-phase signal and quadrature signal) data streams are fed to a Coordinate Rotation Digital Computer (CORDIC) within processor 212, which converts it from Cartesian to polar representation. The resultant amplitude modulation signal is passed through sigma-delta amplitude (SAM) signal processing blocks 214 before they are passed onto the on-chip digital pre-power amplifier (DPA) 234, while the phase modulation output of the cordic is passed onto the ADPLL after the necessary interpolation and signal processing, which performs the phase modulation of the DCO.

[0047] Bandwidth on Demand (BonD) module 260 monitors the amplitude modulation (AM) signal and the phase modulation (PM) signal produced by the CORDIC module. In some embodiments, only the amplitude modulation signal is monitored. As will be described in more detail below, BonD module 260 changes parameters in loop filter 222 to increase loop bandwidth when an impending power spike or sudden change is detected, and then restores the parameters to narrow the loop bandwidth after the power spike has subsided.

[0048] Under no modulation conditions, ADPLL digitally controls the DCO to produce a stable variable clock (CKV) in the targeted RF frequency band. In the feedback path, CKV is used for phase detection and reference retiming. The time to digital phase conversion in the feedback happens using a TDC inverter chain 242.

[0049] The channel and data frequency control words are in the frequency command word (FCW) format, which is defined as the fractional frequency division ratio N, with a fine frequency resolution limited only by the FCW wordlength. For example, with 24 fractional FCW bits, the frequency granularity using a 38.4 MHz reference frequency is 38.4 MHz/2^{24}/2.29 Hz. In this embodiment, the direct point frequency injection is at the CKVD16 (which is 1xHB/2xLB channel frequency divided by 16, i.e., CKVD16=f16/16Hz), so the possible DCO frequency resolution is in the range of 6-7.5 Hz (computed as f1/1624).

[0050] The frequency reference (FREF) clock contains the only reference timing information for the RF frequency synthesizer to which phase and frequency of the RF output are to be synchronized. The RF output frequency (f4) is related to the reference frequency (f0) according to the following formula.

\[ f_4 = N f_0 \]  

[0051] where, \( N = f_4 / f_0 \equiv FCW \).

Synchronous Phase-Domain Operation

[0052] The ADPLL operates in a digitally-synchronous fixed-point phase domain. The variable phase \( R_{4}[k] \) is determined by counting the number of rising clock transitions of the DCO oscillator clock CKV using variable phase accumulator 236. The variable phase \( R_{4}[k] \) is sampled via sampler 238 to yield sampled FREF variable phase \( R_{4}[k] \), where k is the index of the FREF edge activity. The sampled FREF variable phase \( R_{4}[k] \) is fixed-point concatenated with the
normalized time-to-digital converter (TDC) 242 output \( e[k] \). The TDC measures and quantizes the time differences between the frequency reference FREF and the DCO clock edges. The sampled differentiated (via block 240) variable phase is subtracted from the frequency command word (FCW) by a synchronous arithmetic phase detector 218. The reference phase \( \Phi_0[k] \) is conceptually obtained by accumulating FCW with every cycle of the retimed frequency reference (FREF) clock input.

The frequency error \( f_d[k] \) samples are accumulated via the frequency error accumulator 220 to create the phase error \( \Phi_d[k] \) samples. The digital phase error \( \Phi_d[k] \) is filtered by a digital loop filter 222 and then normalized by the DCO gain normalization circuit 270 in order to correct the DCO phase/frequency in a negative feedback manner. The loop behavior due to its digital nature is independent of process, voltage and temperature variations. The FREF retiming quantization error \( e[k] \) is determined by the time-to-digital converter (TDC) 242 and the DCO period normalization multiplier 244. The TDC is built as a simple array of cascaded inverter delay elements and flip-flops, which produces time conversion resolution finer than 25 ps in the design process.

It must be recognized that the two clock domains, FREF and DCO, are not entirely synchronous and it is difficult to physically compare the two digital phase values without having to face metastability problems. During the frequency acquisition, their edge relationship is not known and during the phase lock the edges will exhibit rotation if the fractional FCW is non-zero. Consequently, the digital-word phase comparison is performed in the same clock domain. The synchronous operation is achieved by over-sampling the FREF clock using a higher-rate DCO derived clock (typically CKVD8) in reference retiming circuit 246. The resulting retimed CKR clock is thus stripped of the FREF timing information and is used throughout the system. This ensures that the massive digital logic is clocked after the quiet interval of the phase error detection by the TDC.

The main advantage of representing the phase information in fixed-point digital numbers is that, after the conversion, it cannot be further corrupted by noise. Consequently, the phase detector could be simply realized as an arithmetic subtractor that performs an exact digital operation. Thus, having a single conversion place, where the continuously-valued clock transition edge delay is quantized within the TDC, the susceptibility to noise and quantization errors is minimized and well controlled. It should be emphasized that it is very advantageous to operate in the phase domain for several reasons. First, the phase detector used is not a conventional correlator/multiplier generating reference spurs. DRP architecture uses an arithmetic subtractor 218, which does not introduce any spurs into the loop. Second, the dynamic range of the phase error could be made arbitrarily large simply by increasing the word-length of the phase/frequency accumulators. Conventional three-state phase/frequency detectors are typically limited to only \( \pm \pi \) of the comparison range. Third, the phase domain operation is more amenable to digital implementations, contrary to the conventional approach.

**High-Speed Direct Frequency Modulation Capability**

As shown in FIG. 3, the oscillating frequency deviation \( \Delta f \) is dynamically controlled by directly modulating the DCO frequency in a feed-forward manner. The ADPLL loop compensates by effectively removing the loop dynamics from the modulating transmit path (using the reference modulation injection). The remainder of the loop, including all error sources, operates under the normal closed-loop regime. This method is similar to the conventional two-point direct modulation scheme but because of the digital nature, it is exact and does not require any analog component matching, except for the DCO gain \( K_{DCO} \). A frequency calibration, which is achieved in using a robust hybrid stochastic-gradient algorithm implemented in digital domain, where OTW is the oscillator tuning word and is analogous to the voltage tuning of a VCO.

**Advantages of Using Higher Rate Direct-Point Modulation Injection**

One of the key advantages of using a direct point injection rate (say of channel frequency divided by 16) is that the phase modulation can be presented to the DCO with a finer resolution. For example, the phase modulation in GSM has a BW of 200.00 kHz, while for a polar TX, in EDGE mode the phase modulation BW is approx. 0.0 MHz (LB) and 1.0 MHz (HB). The CKVD16 rate corresponds to an injection frequency range of 103-124 MHz, which is at least three times higher than an FREF of 38.4 MHz, and 4 times higher than an FREF of 26 MHz. This implies that the phase modulation data update using a CKVD16 rate will be 3-4 times finer than the FREF rate used in the previous generations of ADPLL.
signal processing spurs are below the noise floor and can not be seen in realistic simulations or measurements.

Another important benefit of using CKVDx, where x = 16 or 8 for direct point injection is that the quality of phase modulation injection becomes independent of the FRE frequency. The same ADPLL when used with different FRE’s, say 26, 38.4 or 52 MHz will exhibit the same direct point injection fidelity. However, note that there are other noise scaling terms that will be impacted by the FRE frequency change, but the ADPLL loop filters, modulation injection rates, etc. will maintain their resolution across multiple possible reference frequencies.

It has been observed in many of the ADPLL that the current spikes caused by clocking of bulk of the logic can be a source of spurious emissions. This is especially true for highly integrated transceivers targeted using DRP technology. For ADPLL, a significant part of the loop filter and DCO interface logic execute on the LO derived clock domain. Since most of these frequencies are chosen to be higher than FRE, any such parasitic products will have a larger intra-spur distance than FRE. For example, using CKVD32, the spur (if present) will be 52-62 MHz apart as compared to FRE frequencies. In retrospect, the current spikes due to the modulation injection rate into DCO have the highest impact, as the rush current to the boundary level-shifters might be supplied by the same LO supply regulator, which powers DCO. The most critical among these spurs are the ones that appear in the corresponding GSM/EDGE RX band during transmission. The widest GSM RX band is 65 MHz, and using CKVD16 at the interface at most one spur may appear in the RX band due to these parasitic supply regulation issues. Therefore, the use of a higher direct-point injection frequency (>100 MHz) theoretically reduces the possibility of multiple spurs in the RX band.

FIG. 4 is a block diagram of loop filter 222 for the ADPLL of FIG. 3. The loop filter’s main input is the PHASE_ERR signal 1008 output from the RESAMPLER block 256. Its main function is to first filter the phase error signal and then feed the filtered phase error signal to the proportional-integral controller (equivalent of type-II operation in an analog PLL) of the DCO. Note that the applied proportional and integral gains include DCO gain normalization for each of the DCO capacitor banks. The loop filter outputs TUNE_PLL 402, which is the tuning word contribution due to the PLL. This is added (not shown on FIG. 4, but shown on FIG. 3 by adder 224) with TUNE_TX (the feed-forward modulation injection) in the DCO interface (DCOIF) block to produce the composite OTW word (as shown in FIG. 3).

The proportional part 406 of the ADPLL loop has a gain alpha, which is used in both type-I (used for the DCO PVT and Acquisition bank tuning) and type-II (used for DCO tracking bank tuning) operational modes of ADPLL. ADPLL can have different programmable alpha coefficients that can be used based on the operational mode.

The four IIR filters 404 exist to filter the noisy PHASE_ERR or PHE signal. All four IIR stages are similar with following first-order transfer function:

$$\phi(t)[1-e^{-\frac{t}{\tau}}] (1)$$

where lambda is a programmable value and can take any value from 0 to 7.

The integral loop 1194 is intended to only work in tracking mode once the proportional loop is already quite close to the desired channel frequency. This is followed to minimize the overall settling time of ADPLL, otherwise, there is no hardware limitations forcing this to only be used during tracking. By adding an integrator to the loop, the loop will work to zero out the phase error. To prevent this long settling, the integral loop samples the current IIR filtered PHE and uses the result to subtract 408 from subsequent phase error samples. This results in a new offset error signal that can be forced to zero deviation by the integral control. The offset error value is then accumulated by the digital integrator and multiplied by the integral gain, rho, before it is added to the proportional connection.

FIG. 5 represents a simple model of the loop filter to illustrate various dynamic operating possibilities. Filter 502 represents embodiments of filter 222. Oscillator 504 represents oscillator 228. Two cases will be described: 1) a simple proportional-integral (PI) filter, and 2) a PI filter preceded by a set of infinite impulse response (IIR) filters. To compute the dependence of the PLL dynamics on the loop filter parameters, equation 2 represents the general operation of filter 502:

$$\Phi(s)=\Phi(s)\Phi(s)+\Phi(s)\Phi(s)$$

where alpha and rho are the proportional and integral gains of the controller.

In frequency domain, the loop filter transfer function is

$$H(s) = \frac{\Phi(s)}{\Phi(s)}$$

With the oscillator 504 being represented by a simple integrator, i.e.,

$$O(s) = \frac{1}{s}$$

we can write the PLL transfer function as

$$G(s) = \frac{H(s)O(s)}{1+H(s)O(s)}$$

$$= \frac{1}{1+\frac{\alpha+\rho}{\tau}+\frac{\alpha+\rho}{\tau}}$$

$$= \frac{\tau(\alpha+\rho)}{\tau(\alpha+\rho)+1}$$

Comparing the denominator with a generic 2nd order system transfer function, we have

$$s^2+2\sigma+\rho = s^2+2\omega_0\rho\sigma \omega_0$$

Dec. 31, 2009
Comparing coefficients, we get
\[ 2i \omega_o = \alpha \]
\[ \omega_o = \rho \]  
(7)
and simplifying the relations along with the standard relation for frequency response of a 2\textsuperscript{nd} order system
\[ \omega = \omega_o \sqrt{1 - \xi^2} \]
(8)
we have
\[ \omega_o = \sqrt{\rho} \]
\[ \zeta = \frac{\sigma}{2 \sqrt{\rho}} \]
\[ \omega = \sqrt{\rho - \frac{a^2}{4}} \]
(9)
Therefore, for the simple PLL, the settling time of the system is given by
\[ t_s = \frac{4}{\zeta \omega_o} = \frac{8}{a} \]  
(10)
It is evident from (9) and (10) that the key ADPLL parameters such as the damped frequency response, loop bandwidth and phase margin are a function of both PI controller parameters.

Case II
For the case of a type-II PLL, when the loop filter comprises a set of filters followed by a PI controller, as illustrated in FIG. 4, the z-domain transfer function of the ADPLL loop filter 222 is given by
\[ H(z) = aF(z) + \frac{\rho Z^{-1}}{1 - z^{-1}} \]  
(11)
where \( \alpha \) and \( \rho \) are the proportional and integral gains of the controller and \( F(z) \) is the transfer function of the IIR filters given by
\[ F(z) = \sum_{i=0}^{3} \frac{\lambda_i}{1 + (1 - \lambda_i)z^{-1}} \]  
(12)
In s-domain, the corresponding loop filter transfer function is
\[ H(s) = \frac{dF(s)}{ds} = aF(s) + \frac{\rho}{s} \]  
(13)
where \( F(s) \) is the s-domain equivalent transfer function of the IIR filters. Therefore, the ADPLL transfer function becomes
\[ G(s) = \frac{saF(s) + \rho}{s^2 + saF(s) + \rho} \]  
(14)
Comparing the denominator with a generic 2\textsuperscript{nd} order system transfer function, we have
\[ s^2 + saF(s) + \rho = s^2 + 2\omega_o s + \omega_o^2 \]
(15)
Comparing coefficients, and simplifying we get the following relations for the ADPLL dynamics
\[ \omega_o = \sqrt{\rho} \]
\[ \zeta = \frac{\sigma F(s)}{2 \sqrt{\rho}} \]
\[ \omega = \sqrt{\rho - \frac{a^2 F(s)^2}{4}} \]  
(16)
Therefore, for the simple PLL, the settling time of the system is given by
\[ t_s = \frac{4}{\zeta \omega_o} = \frac{8}{a F(s)} \]  
(17)
Therefore the damping factor \( \zeta \) (and hence the phase margin) and the damped frequency response \( \omega \) of the PLL are a function of the PI gain control parameters as well as the transfer function of the filters preceding the proportional gain block.

FIG. 6 shows a z-domain model of the ADPLL, i.e., the input and the output of the ADPLL are in terms of frequency units. The model includes phase detector module 1218, loop filter module 1222, normalized DCO module 602 and feedback TDC/PVL module 604. The loop filter 1222 for ADPLL comprises four independently controlled IIR stages and a proportional-integral (PI) controller. Equation (18) is a linearized z-domain model that includes the four cascaded single-stage IIR filters, each with an attenuation factor \( \lambda_i \), where \( i = 0 \ldots 3 \) as well as the proportional and integral parts of the loop. The loop filter operates at the \( f_{VD} \cdot f_{DC}/32 \) rate, where \( f_{DC} \) is the DCO output frequency.
\[ H_{\text{loop}}(z) = \sigma \cdot \sum_{i=0}^{3} \frac{\lambda_i}{1 + (1 - \lambda_i)z^{-1}} + \frac{\rho Z^{-1}}{1 - z^{-1}} \]  
(18)
Alternately, ADPLL also supports a mode in which the integral part of the PI controller also operates on filtered phase error computed by operating a set of cascaded IIR filters on the resampled PHE signal. The main advantage of this mode is that as the integral part operates on an error signal, which has undergone low pass filtering after resampling (identical to the proportional part) resulting in better group delay equalization of the two paths. Note that in this mode the phase margin of the ADPLL under similar conditions will be sacrificed. In this mode, the loop filter can be expressed as follows:
Note that the coefficients α (alpha) and ρ (rho) control the overall gain of filter 1222. Operation of these two coefficients will be described in more detail below.

\[ H_{DCO}(z) = \frac{\frac{1}{1-z^{-1}}}{\frac{1}{f_{VD}}} \]  

(20)

The simplified feed-forward transfer function of the loop is

\[ H_{FF}(z) = \frac{\frac{1}{1-z^{-1}}}{\frac{1}{f_{R}}} \left( \sum_{n=0}^{N} \frac{\lambda_n}{1+(1-\lambda_n)z^{-1}} \right) \]  

(21)

where \( r \) is the dimensionless ratio representing the DCO gain estimation error.

The transfer function of the feedback components is

\[ H_{FB}(z) = \frac{\frac{1}{1-z^{-1}}}{\frac{1}{f_{R}}}(\frac{1}{1-z^{-1}}) = \frac{z^{-1}}{1-z^{-1}}z^{-4} = \frac{z^{-1}}{f_{R}} \]  

(22)

The closed loop transfer function for the reference is lowpass with the gain multiplier \( N = f_{FV} \), i.e.,

\[ H_{CLREF}(z) = \frac{H_{FF}(z)}{1+H_{FF}(z)H_{FB}(z)} \]  

(23)

The closed loop transfer function for the TDC is lowpass. Neglecting the accumulation and the differentiation operations in the feedback path, we can write the closed-loop transfer function for TDC as

\[ H_{CLTDC}(z) = \frac{H_{FF}(z)}{1+H_{FF}(z)H_{FB}(z)} \]  

(24)

The closed loop transfer function for the direct-point injection into the DCO is highpass in nature and is given by

\[ H_{CLDCO}(z) = \frac{1}{1+H_{FF}(z)H_{FB}(z)} \]  

(25)

FIG. 7 is a block diagram of the ADPLL loop filter 1222 with proportional (alpha) gear-shifting circuit 702 and integral (rho) gear shifting circuit 704. The amplitude and phase transfer function differences using the ADPLL loop filters in the configurations as captured in Eq. 18 and 19 impacts the ADPLL closed loop performance as well. Note that all the transfer functions are a function of the DCO frequency \( f_{VD} \) or its derivatives, such as \( f_{VD} \).

The primary advantage of operating the ADPLL on the \( f_{VD} \) frequency is the improved spectrum and better rejection of the reference spurs. However, this results in the ADPLL loop response to vary as a function of DCO frequency for fixed ADPLL tuning parameters. Although this ADPLL BW variation is quite small, it can be taken care of by optimal tuning of the ADPLL loop parameters as a function of the DCO output frequency. Note that for the entire GSM/EDGE tuning range this variation is less than 4% of PLL BW and less than 2% of the ADPLL phase margin.

Some operating points computed for GSM modulation using the model presented in equations 18–25 are shown in Table 1. The coefficients are power-of-two exponents.

<p>| Table 1 |
| ADPLL Loop Parameters - Channel Frequency = 1800 MHz |</p>
<table>
<thead>
<tr>
<th>lambda1</th>
<th>lambda2</th>
<th>lambda3</th>
<th>lambda4</th>
<th>alpha</th>
<th>rho</th>
<th>0 dB loop BW [kHz]</th>
<th>Gain Margin [dB]</th>
<th>Phase Margin [deg]</th>
<th>50 kHz Loop Gain [dB]</th>
<th>400 kHz Loop Gain [dB]</th>
<th>3 MHz Loop Gain [dB]</th>
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<tbody>
<tr>
<td>4</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>8</td>
<td>18</td>
<td>15.57</td>
<td>17.64</td>
<td>45.00</td>
<td>-10.22</td>
<td>-66.53</td>
<td>-98.31</td>
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<td>2</td>
<td>4</td>
<td>4</td>
<td>6</td>
<td>7</td>
<td>16</td>
<td>30.89</td>
<td>20.28</td>
<td>45.23</td>
<td>-2.04</td>
<td>-36.02</td>
<td>-87.14</td>
</tr>
<tr>
<td>5</td>
<td>6</td>
<td>2</td>
<td>7</td>
<td>16</td>
<td>30.87</td>
<td>20.28</td>
<td>45.23</td>
<td>-2.04</td>
<td>-36.02</td>
<td>-87.14</td>
<td>-93.12</td>
</tr>
<tr>
<td>3</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>7</td>
<td>16</td>
<td>31.15</td>
<td>17.38</td>
<td>44.81</td>
<td>-1.70</td>
<td>-38.27</td>
<td>-86.31</td>
</tr>
<tr>
<td>1</td>
<td>5</td>
<td>6</td>
<td>6</td>
<td>19</td>
<td>44.16</td>
<td>9.96</td>
<td>45.48</td>
<td>2.53</td>
<td>-41.59</td>
<td>-106.55</td>
<td>-91.12</td>
</tr>
<tr>
<td>1</td>
<td>3</td>
<td>4</td>
<td>6</td>
<td>15</td>
<td>54.24</td>
<td>16.08</td>
<td>45.30</td>
<td>2.60</td>
<td>-28.40</td>
<td>-85.65</td>
<td>-91.12</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>5</td>
<td>0</td>
<td>6</td>
<td>14</td>
<td>61.66</td>
<td>20.02</td>
<td>45.10</td>
<td>3.36</td>
<td>-21.80</td>
<td>-86.01</td>
</tr>
</tbody>
</table>
Proportional and Integral Gain Gear Shifting

[0089] An important issue in frequency synthesis for today’s wireless applications is the acquisition or settling time to a new channel frequency from the trigger event to the instance when the wireless terminal is ready to transmit or receive with the specified low level of frequency error, phase noise and spurious tones.

[0090] The gain of ADPLL control loop requires special settings for different modes of operation. Gear shifting changes the gain of the control loop to suit the various operating modes. For example, it is desirable to have high loop bandwidth while initially locking in acquisition mode in order that the PLL settle quickly. In tracking mode, however, it is desirable to have a low loop bandwidth to increase the performance of the PLL. Increasing the loop gain widens the bandwidth of the PLL while decreasing the loop gain narrows the loop bandwidth.

[0091] Both the proportional and integral loops have the capability to change their bandwidths via gear shifting. The proportional loop is controlled by coefficient alpha (alpha), while the integral loop is controlled by coefficient rho (rho). When a gear shift occurs, the gear shift value increments (or decrements) the corresponding gain. A gear shift mechanism is described in more detail in U.S. Pat. No. 7,498,890 entitled “CONTINUOUS REVERSIBLE GEAR SHIFTING MECHANISM” and which is incorporated by reference herein in its entirety.

[0092] Both alpha and rho together affect the bandwidth or more particularly, frequency response, of the ADPLL. In the IIR gear shift block, the IIR filter is unity gain. Unity gain is defined as a gain of linear 1 or 0 dB at DC when clocked continuously. The lambda (λ) coefficients, however, can be changed without negative implications to the operation of the gear shift mechanism or loop performance.

[0093] With reference to the proportional alpha gear shift mechanism 702, alpha and gain (g) are multiplied together to provide an effective alpha. The gear shifting is effected in this manner whereby the feed forward gain is changed without generating a DC perturbation to the system.

[0094] With reference to the integral rho gear shift block 704, register 712 and adder 714 function as an integrator to accumulate the p gain. The p gear shift is operative to accumulate the unfiltered phase error 706 or filtered phase error 708 and multiply the result by the value rho. This changes the dynamics of the loop from type-I to type-II operation. A type-I is an integrator-free system (the only integrator would be the DCO) wherein loop operation is proportional. A type-II loop has an integrator in its loop. A type-I loop is used when better noise performance is desired, especially removal of the DCO flicker noise.

[0095] When operating in a type I loop, the alpha gear shifting is sufficient since the integral portion (i.e., the rho gear shift) is not active. When the loop moves to a type II operation, both the alpha and the rho coefficients must be changed simultaneously to effect a gear shifting of the loop bandwidth without substantially changing the frequency response shape (only scaling would be preferred) and without negatively affecting the loop stability, such as gain or phase margins, or damping factor for type-II second-order systems.

[0096] For the dynamic proportional gain gear-shifting, the feedback register 710 needs to sample a new value for the feedback path. Gear shifting can occur during any of the ADPLL operational modes; however, it is currently most useful for during tracking and for bandwidth on demand in response to predicted DCO pulling. Although the ADPLL loop bandwidth can be adjusted independently using either proportional (coarse change) or integral (finer change) gains, the possibility to simultaneously gear-shift both alpha and rho allows the ADPLL loop bandwidth to change while maintaining the phase and stability margins for the loop.

[0097] Gear-shifting a PLL implies a dynamically change of the PLL loop parameters such as loop gain, loop bandwidth, etc. However, for an ADPLL with filter as described in eq. 11, the loop parameters are a function of all the loop filter components that includes the parameters for the filtering and proportional-integral regulator. Using equation 16, it is clear that for the specific loop filter configuration shown, the ADPLL damping ratio is directly proportional to the proportional gain alpha and the cascaded IIR filter transfer function F(s), while it is inversely proportional to the square root of the integral gain rho. Therefore, if the loop parameters are to be changed while preserving the phase margin of the ADPLL, then all the aforementioned parameters need to be gear-shifted (or switched) simultaneously.

[0098] A set of examples have been provided below for selective ADPLL parameter gear-shifts, that show the dependence of ADPLL loop BW and phase margin on the IIR co-efficient and PI controller gains. Please note that all the loop filter coefficients have been implemented as 2^n coefficients, where n is as specified in the tables below, such that, if n1>n2, then 2^n1<2^n2.

Case A: Gear-Shifting of IIR Filter(s)

[0099] In Table 2, one of the IIR filter coefficients has been decremented, resulting in slight widening of the IIR filter transfer function. As expected from the above equations, this results in the reduction of the ADPLL loop BW, while increasing the gain and phase margin of the system.
Case B: Gear-Shifting of PI Controller’s Proportional Gain

Table 3 shows the impact of gear-shifting the proportional gain $\alpha$ down by one step. The impact is a big increase in the ADPLL loop BW, accompanied with a sharp decline in the gain and the phase margin of the system.

<table>
<thead>
<tr>
<th>$\lambda_1$</th>
<th>$\lambda_2$</th>
<th>$\lambda_3$</th>
<th>$\lambda_4$</th>
<th>$\alpha$</th>
<th>$\rho$</th>
<th>$0 \text{ dB CL BW [kHz]}$</th>
<th>Gain Margin [dB]</th>
<th>Phase Margin [deg]</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>4</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>15</td>
<td>125.99</td>
<td>11.29</td>
<td>44.34</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>15</td>
<td>122.08</td>
<td>12.19</td>
<td>46.09</td>
</tr>
</tbody>
</table>

Case C: Gear-Shifting of PI Controller’s Integral Gain

Table 4 shows the impact of gear-shifting the integral gain $\rho$ up by one step. The impact is a decrease in the ADPLL loop BW, accompanied by an increase in the gain and the phase margin of the system.

<table>
<thead>
<tr>
<th>$\lambda_1$</th>
<th>$\lambda_2$</th>
<th>$\lambda_3$</th>
<th>$\lambda_4$</th>
<th>$\alpha$</th>
<th>$\rho$</th>
<th>$0 \text{ dB CL BW [kHz]}$</th>
<th>Gain Margin [dB]</th>
<th>Phase Margin [deg]</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>4</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>15</td>
<td>125.99</td>
<td>11.29</td>
<td>44.34</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>16</td>
<td>211.64</td>
<td>5.78</td>
<td>28.74</td>
</tr>
</tbody>
</table>

Case D: Simultaneous Gear-Shifting of the PI Controller’s Proportional and Integral Gains

According to equation 9, if we neglect the contribution of the IIR filters, the ADPLL frequency damping and the damping ratio impacting the ADPLL loop BW and the phase margin is proportional to

$$ \frac{\alpha}{2 \sqrt{\rho}}.$$

Therefore, if we gear-shift $\alpha$ up by a factor of 2 (i.e., we gear shift $\alpha$ from 6 to 5, so $2 \times (-5) = -10$, then corresponding the integral gain $\rho$ will need to be gear-shifted by 4. However, when we do so, we observe that the PLL loop BW has scaled by approximately a factor of 2 as expected, however, the phase margin did not hold and shows severe degradation as shown in Table 5.

<table>
<thead>
<tr>
<th>$\lambda_1$</th>
<th>$\lambda_2$</th>
<th>$\lambda_3$</th>
<th>$\lambda_4$</th>
<th>$\alpha$</th>
<th>$\rho$</th>
<th>$0 \text{ dB CL BW [kHz]}$</th>
<th>Gain Margin [dB]</th>
<th>Phase Margin [deg]</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>4</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>15</td>
<td>125.99</td>
<td>11.29</td>
<td>44.34</td>
</tr>
<tr>
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<td>4</td>
<td>4</td>
<td>5</td>
<td>5</td>
<td>13</td>
<td>229.99</td>
<td>4.33</td>
<td>17.85</td>
</tr>
</tbody>
</table>
Case E: Two-Step Gear-Shifting of the IIR and PI Controller Gains

[0103] While the above discussions suggest switching all parameters together is beneficial, it may be useful to have a gear-shifting sequence in which alpha and rho gear-shift together, while the IIRs switch separately in two steps. In this embodiment the alpha/rho are gear-shifted, while the filter coefficients may have switchable settings. Operating this way, the system can still maintain the phase margin to better than approximately 40 degrees. The dwell time on the intermediate setting (with slightly narrower loop BW) is small and does not degrade the PLL system performance. The example in Table 6 shows gear-shifting from narrow to wider loop BW and the sequence gets reversed when switching to wider loop BW.

<table>
<thead>
<tr>
<th>lambda1</th>
<th>lambda2</th>
<th>lambda3</th>
<th>lambda4</th>
<th>alpha</th>
<th>rho</th>
<th>Gain Margin [dB]</th>
<th>Phase Margin [deg]</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>4</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>15</td>
<td>125.99</td>
<td>11.29</td>
</tr>
<tr>
<td>0</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>15</td>
<td>168.43</td>
<td>14.87</td>
</tr>
<tr>
<td>0</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>5</td>
<td>20</td>
<td>206.66</td>
<td>9.75</td>
</tr>
</tbody>
</table>

Case F: Simultaneous Gear-Shifting of the IIR and PI Controller Gains

[0104] Table 7 shows that if we simultaneously gear-shift the ADPLL’s PI controller parameters, while switching the IIR filter coefficients, we can change the ADPLL loop BW while maintaining adequate phase margin. The possible range of gain margin decreases whenever the loop BW is increased as expected for a type-II or higher system. However, note that using the simultaneous switching of IIR filter co-efficients and PI controller parameters, the system can gear-shift between a large set of loop bandwidths, while achieving good gain and phase margins. For good operation, maintaining the bandwidth margin above about 40 degrees provides good results. Some such examples have been presented in Table 7.

<table>
<thead>
<tr>
<th>lambda1</th>
<th>lambda2</th>
<th>lambda3</th>
<th>lambda4</th>
<th>alpha</th>
<th>rho</th>
<th>Gain Margin [dB]</th>
<th>Phase Margin [deg]</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>4</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>15</td>
<td>125.99</td>
<td>11.29</td>
</tr>
<tr>
<td>0</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>15</td>
<td>168.43</td>
<td>14.87</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>4</td>
<td>6</td>
<td>7</td>
<td>16</td>
<td>61.19</td>
<td>16.58</td>
</tr>
</tbody>
</table>

[0105] FIG. 8 is a block diagram of another embodiment illustrative of a way to perform gear shifting in loop filter 222. Multipliers 802 and 804 introduce alpha and rho coefficients, respectively, into the filter process. Multipliers 806 and 808 insert a common \( \alpha_1 \) coefficient as indicated. The multipliers are advantageously realized as bit shift operators for power-of-two multiplying coefficients. The common \( \alpha_1 \) multiplier ensures that alpha and rho maintain the square-root relationship, which maintains the damping factor zeta, as discussed above.

[0106] FIG. 9 is a block diagram of bandwidth on demand (BonD) circuitry 900 to detect and initiate bandwidth on demand in the ADPLL. FIG. 9 illustrates one embodiment of bandwidth on demand detecting circuitry as illustrated by BonD module 260 of FIG. 3. As mentioned earlier, the complex vector modulation I/Q (in-phase signal and quadrature signal) data streams are fed to a COordinate Rotation Digital Computer (CORDIC) within processor 212 (see FIG. 3), which converts it from Cartesian to polar representation. The resulting amplitude modulation signal 902 is passed through sigma-delta amplitude (SAM) signal processing blocks 214 before they are passed onto the on-chip digital pre-power amplifier (DPA) 234, while the phase modulation output of the Cordic is passed onto the ADPLL after the necessary interpolation and signal processing, which performs the phase modulation of the DCO.

[0107] BonD module 900 also monitors amplitude modulation signal 902. It may scale the signal via multiplier 904 in response to control signals from the script processor. It then takes a first derivative 906 and a second derivative 908 to determine the rate of change in amplitude and the acceleration of the change in amplitude, respectively. Multiplexors 910 allow selection of any of the three indicators in response to control signals from the script processor. One selected indicator is compared against a first threshold 912 and the other selected indicator is selected against a second threshold 914. Both thresholds are set based on a parameter provided by the script processor. A timer 916 is also started when one of the thresholds is crossed, if enabled by the script processor. A set of multiplexors and gates, generally indicated at 920, under control of enable signals controlled by the script processor then combines the results of the threshold comparisons and the timer and generates a BonD control signal 930 that is used to cause one or more parameters of the loop filter to be changed to thereby change the loop bandwidth.

[0108] For example, BonD circuitry 900 can be set up by the script processor to detect when the amplitude modulation signal or a derivative of the amplitude signal crosses the first threshold and to then cause an increase in loop bandwidth by asserting control signal 930. After a short period of time determined by the counter, BonD can then cause a decrease in the loop bandwidth by de-asserting control signal 930.

[0109] Alternatively, BonD circuitry 900 can be set up by the script processor to detect when the amplitude modulation
signal or a derivative crosses the first threshold and to then cause an increase in loop bandwidth by asserting control signal 930. After the selected signal indicator falls below the first threshold, BonD can then cause a decrease in the loop bandwidth by de-asserting control signal 930.

[0110] Alternatively, BonD circuitry 900 can be set up by the script processor to detect when the amplitude modulation signal or a derivative crosses the first threshold and to then cause an increase in loop bandwidth by asserting control signal 930. After the selected signal indicator falls below the second threshold, BonD can then cause a decrease in the loop bandwidth by de-asserting control signal 930.

[0111] As can be seen, there is a large number of possibilities that can be configured using configurable BonD circuit 900 to monitor the amplitude modulation signal and to change parameters in the loop filter to increase loop bandwidth when the amplitude signal is changing in value in a significant manner. The change in value of the amplitude signal is what causes the power consumption of the pre-amplifier to change and to thereby cause pulling of the DCO frequency. The amplitude signal has returned to a more steady-state value, BonD circuitry 900 can then sense this condition, either by threshold or by time delay, and reduce the loop bandwidth.

[0112] In a similar manner, BonD 900 may also be embodied in a manner that the phase modulation signal from the CORDIC is also monitored. By taking a derivative of the phase modulation signal, a significant difference in phase can be detected and loop bandwidth increased for a short period of time. In wide bandwidth polar modulation (e.g., EDGE, WCDMA, WLAN, HSUPA, LTE, etc.), the frequency modulation signal exhibits large frequency modulation requirements, due to the complex constellation either approaching or passing through the origin. Such large instantaneous modulation spikes in FM (or a change of instantaneous phase), causes a change in the oscillator output impedance, which has a measurable impact on the quality (or fidelity) of PLL lock. In such cases, the PLL BW can be widened as a function of the instantaneous frequency modulation that the PLL is being modulated with.

[0113] FIG. 10 is a state diagram illustrating state transitions from a narrow bandwidth filter state 3002 to a wide bandwidth filter state 3004 and vice versa in response to the BonD control signal 930 being asserted and de-asserted. ADPLL loop bandwidth (BW) switching is typically triggered in anticipation of events and/or disturbances that potentially impact the quality of the locked local oscillator clock generated by the ADPLL and the DCO system. When bandwidth on demand is enabled in this embodiment, changes are made in response to detecting that an amplitude of the transmission symbols, a derivative of amplitude, or a derivative of phase of the transmission symbols has crossed a threshold, as discussed above. Depending on operating conditions and current coefficient settings, the transition may be made by changing the IIR coefficients and the proportional-integral coefficients α and ρ all simultaneously in state 3006 or state in 3016. The transition may also be made by changing only α and ρ simultaneously in state 308 or in state 3014. In other cases, the transition may be made by changing only the IIR coefficients in state 3010 or in state 3012. Alternatively, in some conditions the transition may be made by first changing only α and ρ simultaneously in state 308 or in state 3014 and then jumping to state 3010 or 3012 respectively to change one or more IIR coefficients. Likewise, the transition can be made via state 3010 to state 3008 or state 3012 to state 3014.

[0114] FIG. 11 is a block diagram of another embodiment of a BonD circuit 1100 to detect and initiate bandwidth on demand in the ADPLL. BonD module 1100 also monitors amplitude modulation signal 902. It then takes a first derivative 1104 and a second derivative 1106 to determine the rate of change in amplitude and the acceleration of the change in amplitude, respectively. In some embodiments, the phase modulation signal 1103 from the CORDIC is also monitored. By taking a derivative 1108 of the phase modulation signal, a significant difference in phase can be detected. Multiplexors 1108 allows selection of any of the various indicators in response to control signals from the script processor. Another indicator that may be monitored in some embodiments is a filtered version of the amplitude modulation signal DTX_ACW APC from DTX module 250. The selected first indicator is compared against a first threshold in comparator 1110 that asserts its output signal ABOVE_TRUE when the first threshold is exceeded. The selected second indicator is also compared against a second threshold in comparator 1112 that asserts its output signal BELOW_TRUE when the selected indicator is less than the second threshold. The thresholds may be configured to be the same or different. The thresholds are set based on parameters provided by the script processor. A timer 1114 is also started in response to a control signal from state-machine 1116. The timer is based on CKVD128 clock rate (12.6 to 15.6 MHz). Its maximum delay at the highest clock rate is about 16 us. State-machine 1116 under control of enable signals controlled by the script processor then combines the results of the threshold comparisons and the timer and generates a HW_GEARSHIFT_WIDE control signal. This signal is then delayed by a programmable delay circuit 1120. Delay circuit 1120 is based on CDVD32 clock rate (50 to 62 MHz). Its maximum delay at highest clock rate is about 4 μs. This allows the adjustment to the loop bandwidth to be delayed by a programmable delay when either threshold is crossed or after the time delay interval. This programmable delay is used to account for any delay or mismatch between a transmission symbol being detected and its actual affect on the DCO. Typically, the amount of the programmable delay would be determined by testing or by simulation of a complete design.

[0115] The output of delay logic 1130 produces BonD control signal 1130 that is used to cause one or more parameters of the loop filter to be changed to thereby change the loop bandwidth. When asserted, the loop filter is changed to wide bandwidth mode and when de-asserted the loop filter is changed to narrow bandwidth mode. The transition from wide to narrow and from narrow to wide may be performed according to the state diagram of FIG. 10.

[0116] Table 8 and Table 9 illustrate an embodiment of two control registers that may be accessed by the script processor to control the thresholds and the operation of the BonD circuit, respectively.
TABLE 8

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function</th>
<th>Value at reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16 mem_bond_thrsh_high</td>
<td>This 16-bits sign number is used to set the higher threshold value of Bond functionality</td>
<td>“0001_1001_0101_0000”</td>
</tr>
<tr>
<td>15:0 mem_bond_thrsh_low</td>
<td>This 16-bits sign number is used to set the lower threshold value of Bond functionality</td>
<td>“0000_1001_0000_0000”</td>
</tr>
</tbody>
</table>

TABLE 9

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function</th>
<th>Value at reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24 mem_bond_delay</td>
<td>Value of this register is used to delay the output of DTX_BOND state machine to DLO by kvd32 clock cycles if mem_bond_delay_en is set to ‘1’</td>
<td>“00000000”</td>
</tr>
<tr>
<td>23:16 mem_bond_timer</td>
<td>Value of this register is used to control the duration (number of CKVD128 cycles) of DLO gear shifting when output of either threshold comparators is true.</td>
<td>“00110000”</td>
</tr>
<tr>
<td>15:11 NU</td>
<td></td>
<td>“0”</td>
</tr>
<tr>
<td>10:10 mem_bond_delay_en</td>
<td>If set to ‘1’ then value of mem_bond_delay register issued delay the output of Bond State machine to DLO.</td>
<td>“00000000”</td>
</tr>
<tr>
<td>9:0 mem_bond_mode</td>
<td>These bits are used to control the DTX BOND functionality</td>
<td>“00000000”</td>
</tr>
<tr>
<td></td>
<td>Bit(0) = If set to ‘1’ DTX Bond Hardware is enabled.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit(1) = This bits control DTX BOND operation if</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit(0) is ‘1’, ‘0’ =&gt; Simple Mode, ‘1’ =&gt; Complex Mode</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit(2) = If set to ‘1’ output of DTX Bond is controlled by Bit(3); if set to ‘0’ Bond State Machine controls the DTX Bond output.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit(3) = Value of this bit is assigned to DTX BOND output if Bit(2) is set to ‘1’.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit(5:4) = These bits are used to control the input to the Higher Threshold Comparator; 00 =&gt; Output of Edge Cordic block</td>
<td></td>
</tr>
<tr>
<td></td>
<td>01 =&gt; Output of Edge APC block</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10 =&gt; First order differentiation of Edge APC output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>11 =&gt; Second order differentiation of Edge APC output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit(7:6) = These bits are used to control the input to the Lower Threshold Comparator; 00 =&gt; Output of Edge Cordic block</td>
<td></td>
</tr>
<tr>
<td></td>
<td>01 =&gt; Output of Edge APC block</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10 =&gt; First order differentiation of Edge APC output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>11 =&gt; Second order differentiation of Edge APC output</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit(8) = If set to ‘1’ output of Higher Threshold Comparator is inverted.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit(9) = If set to ‘1’ output of Lower Threshold Comparator is inverted.</td>
<td></td>
</tr>
</tbody>
</table>

[0117] FIG. 12 is a state diagram illustrating operation of the bandwidth on demand controller of FIG. 11. When BondD mode is enabled by the script processor, comparator outputs are monitored during the IDLE state. During the IDLE state, BondD control signal 1130 is de-asserted to maintain the loop bandwidth in narrow mode. When the ABOVE_TRUE signal is asserted in response to a selected indicator crossing a threshold, the ABOVE_S1 state is entered, and when the BELOW_TRUE signal is asserted, the BELOW_S1 is entered. During each of states S1, S2, S3, and S4 the BondD control signal 1130 is asserted to cause one or more parameters of the loop filter to be changed to thereby change the loop bandwidth to wide mode. State S1 also asserts the TIMER_START signal and then transitions to state S2. If not in complex mode, as configured by the script processor, the state machine stays in S2 until the timer expires and then goes to state S4 where BondD signal 1130 is de-asserted to cause the loop filter to be changed to narrow bandwidth mode. Once the ABOVE_TRUE or BELOW_TRUE signal is de-asserted, the state machine returns to IDLE.

[0118] If the script processor has configured the complex mode, then state S3 is entered from state S4 when the ABOVE_TRUE or BELOW_TRUE signal is de-asserted. Similarly, if the ABOVE_TRUE or BELOW_TRUE signal is de-asserted before the timer expires, then state S3 is entered from state S2. State S3 restarts the timer and then transitions to state S5. If in ABOVE_S5, then the state machine will
transition to IDLE if the timer expires; or transition to 
ABOVE_SI if the ABOVE_TRUE signal is asserted; or transition to 
BELOW_SI if the BELOW_TRUE signal is asserted. Similarly, if in 
BELOW_SS, then the state machine will transition to IDLE if the timer expires; or transition to 
BELOW_SI if the BELOW_TRUE signal is asserted; or transition to 
ABOVE_SI if the ABOVE_TRUE signal is asserted.

[0119] In this manner, the BonD control signal can cause 
the loop filter to be changed to wide bandwidth mode when a 
threshold is crossed and remain in wide mode for a timed 
period. If the other threshold is crossed before the timer 
expires, then wide bandwidth mode will be retained for 
another period of time until the timer expires, at which time 
the loop filter will be changed to reestablish narrow 
bandwidth mode.

[0120] Typically, a particular system will be tested and the 
script processor will be programmed to select the mode of 
operation, the thresholds and time durations that produce the 
best result over a range of conditions.

[0121] FIG. 13 is a plot of modulation spectrum vs attenuation 
in the ADPLL at 400 kHz. This plot illustrates the effect 
on bandwidth which rises as loop attenuation is reduced.

[0122] FIG. 14 is a plot illustrating modulation spectrum vs 
percentage of wide bandwidth time at 400 kHz. This plot 
illustrates the effective average spectrum changes from 0% 
BonD duration to 100% wide bandwidth duration.

[0123] FIG. 15 is a block diagram of mobile cellular phone 
for use in the network of FIG. 1. Digital baseband 
(DBB) unit 1002 can include a digital processing processor 
system (DSP) that includes embedded memory and security 
features. Stimulus Processing (SP) unit 1004 receives a voice 
stream from handset microphone 1013a and sends a voice 
stream to headset mono speaker 1013b. SP unit 1004 
also receives a voice data stream from microphone 
1014a and sends a voice data stream to mono headset 1014b. 
Usually, SP and DBB are separate ICs. In most embodiments, 
SP does not embed a programmable processor core, but performs 
processing based on configuration of audio paths, filters, 
gains, etc being setup by software running on the DBB. 
In an alternate embodiment, SP processing is performed on 
the same processor that performs DBB processing. In another 
embodiment, a separate DSP or other type of processor performs 
SP processing.

[0124] In this embodiment, the digital base band 
processing is included in a single integrated circuit chip with the 
transceiver in the form of a DRPu as a system on a chip (SOC).

[0125] RF transceiver 1106 is a digital radio processor and 
includes a receiver for receiving a stream of coded data 
frames from a cellular base station via antenna 1107 and a 
transmitter for transmitting a stream of coded data frames to 
the cellular base station via antenna 1107. At the heart of 
transceiver 1106 lies a digitally controlled oscillator (DCO), 
which deliberately avoids any analog tuning controls. Fine 
frequency resolution is achieved through high-speed dithering 
of its varactors. Digital logic built around the DCO realizes 
an interpolative all-digital PLL (ADPLL) that is used as a 
local oscillator for both the transmitter and receiver and operates as described above. The polar transmitter architecture 
utilizes the wideband direct frequency modulation capability 
of the ADPLL and a digitally controlled power amplifier (DPA) for the power ramp and amplitude modulation. In this embodiment, a single transceiver supports both GSM and 
WCDMA operation but other embodiments may use multiple 
transceivers for different transmission standards. Other 
embodiments may have transceivers for a later developed 
transmission standard with appropriate configuration. RF 
transceiver 1106 is connected to DBB 1102 which provides 
processing of the frames of encoded data being received and 
transmitted by cell phone 1100.

[0126] The basic WCDMA DSP radio consists of control 
and data channels, rake energy correlations, path selection, 
rake decoding, and radio feedback. Interference estimation 
and path selection is performed by instructions stored in 
memory 1112 and executed by DBB 1102 in response to 
signals received by transceiver 1106. Programmable features 
of the ADPLL within transceiver 1106 are controlled by 
instructions executed by DBB 1102.

[0127] Embodiments of the present invention minimize 
signal quality degradation incurred due to pulling of the oscil­
lator by noise or ground bounce caused by transients in amplit­
tude modulation. In the current embodiment of the ADPLL 
arhitecture, which is strictly optimized for low area and 
power consumption, maintaining an excessive ADPLL band­
width all the time in order to manage noise induced oscillator 
pulling would degrade spectral mask by less filtering of the 
reference and TDC (time to digital converter) phase noise. 
Embodiments of the present invention dynamically increase the 
ADPLL loop bandwidth only when it is really needed. 
During the course of modulation, the significant pulling force 
exists only for a fraction of the time. Therefore most of the 
time it is not strong enough to create a noticeable degradation in error vector magnitude (EVM). Engaging a wide ADPLL 
broadband only at the time of strong frequency pulling miti­
gates its negative effects and leads to only a small increase in the 
close-in phase noise, as described in more detail above. 
For example, if the duty cycle of the wide bandwidth is 50% 
then the resultant modulation spectrum will be midway 
between that of the normal bandwidth and wide bandwidth. 
Typically, the wide bandwidth duty cycle will be much less than 50%.

[0128] DBB unit 1002 may send or receive data to various 
achines connected to universal serial bus (USB) port 1026. 
BBS 1002 can be connected to subscriber identity module 
(SIM) card 1010 and stores and retrieves information used for 
making calls via the cellular system. DBB 1002 can also 
connected to memory 1012 that augments the onboard 
memory and is used for various processing needs. DBB 1002 
can be connected to Bluetooth baseband unit 1030 for wire­
less connection to a microphone 1032a and headset 1032b for 
sending and receiving voice data. DBB 1002 can also be 
connected to display 1020 and can send information to it for 
interaction with a user of the mobile UE 1000 during a call 
rocess. Display 1020 may also display pictures received from 
the network, from a local camera 1026, or from other 
rices such as USB 1026. DBB 1002 may also send a video 
stream to display 1020 that is received from various sources 
such as the cellular network via RF transceiver 1006 or camera 
1026. DBB 1002 may also send a video stream to an 
eternal video display unit via encoder 1022 over composite 
output terminal 1024. Encoder unit 1022 can provide encod­
ing according to PAL/SECAM/NTSC video standards. In 
embodyments, audio codec 1109 receives an audio 
stream from FM Radio tuner 1108 and sends an audio stream 
to stereo headset 1116 and/or stereo speakers 1118. In other
embodiments, there may be other sources of an audio stream, such a compact disc (CD) player, a solid state memory module, etc.

Other Embodiments

[0129] While the invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various other embodiments of the invention will be apparent to persons skilled in the art upon reference to this description.

[0130] In another embodiment, the BonD module may monitor other indicators of frequency pulling. The pulling of the oscillator manifests itself as a degradation of RMS or peak phase error in the PLL. It also causes a degradation of TX close-in performance such as error vector magnitude (EVM), degradation or degraded adjacent channel leakage. For power aggressors, the coupling may correspond to envelope (or amplitude) squared, or their derivatives.

[0131] Various configurations of the BonD circuit and the controlling state machines were illustrated. In other embodiments, the detection circuit may be limited to only one or a few indicators. Other arrangements of the state machines may be used.

[0132] In another embodiment, parameters used for the IIR filters, alpha and rho may take on different values than were illustrated herein, based on a particular design, operating frequency(s) and voltages, design of a particular integrated circuit, and so on. Testing of production units may result in a final selection of parameters to use for the adjustment of bandwidth on demand.

[0133] While the invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various other embodiments of the invention will be apparent to persons skilled in the art upon reference to this description. This invention applies to all scheduled communication systems which use digitally controlled oscillators. This invention applies in uplink and downlink. Various embodiments of the invention are available for many modulation strategies, which include but are not limited to, OFDMA, CDMA, DFT-spread FDMA, SC-OFDMA, and others. Embodiments of this invention can be applied in most if not all emerging wireless standards, including EUTRA.

[0134] While a mobile user equipment device has been described, embodiments of the invention are not limited to mobile devices. Desktop equipment and other stationary equipment being served by a cellular network may also embody an ADPLL as described herein.

[0135] Although the invention finds particular application to Digital Signal Processors (DSPs), implemented, for example, in an Application Specific Integrated Circuit (ASIC), it also finds application to other forms of processors. An ASIC may contain one or more megacells which each include custom designed functional circuits combined with pre-designed functional circuits provided by a design library.

[0136] An embodiment of the invention may include a system with a processor coupled to a computer readable medium in which a software program is stored that contains instructions that when executed by the processor perform the functions of modules and circuits described herein. The computer readable medium may be memory storage such as dynamic random access memory (DRAM), static RAM (SRAM), read only memory (ROM), Programmable ROM (PROM), erasable PROM (EPROM) or other similar types of memory. The computer readable media may also be in the form of magnetic, optical, semiconductor or other types of discs or other portable memory devices that can be used to distribute the software for downloading to a system for execution by a processor. The computer readable media may also be in the form of magnetic, optical, semiconductor or other types of disc unit coupled to a system that can store the software for downloading or for direct execution by a processor.

[0137] As used herein, the terms “applied,” “connected,” and “connection” mean electrically connected, including where additional elements may be in the electrical connection path. “Associated” means a controlling relationship, such as a memory resource that is controlled by an associated port. The terms assert, assertion, de-assert, de-assertion, negate and negation are used to avoid confusion when dealing with a mixture of active high and active low signals. Assert and assertion are used to indicate that a signal is rendered active, or logically true. De-assert, de-assertion, negate, and negation are used to indicate that a signal is rendered inactive, or logically false.

[0138] It is therefore contemplated that the appended claims will cover any such modifications of the embodiments as fall within the true scope and spirit of the invention. What is claimed is:

1. A system, comprising a transmitter, wherein the transmitter comprises:

   a phase locked loop (PLL) having a dynamically controllable loop bandwidth, the PLL comprising an oscillator; a transmit modulator coupled to the PLL for performing vector modulation in response to transmission symbols, wherein each transmission symbol comprises an amplitude signal and a phase signal; and a controller coupled to the PLL and to the transmit modulator operable to detect when a criteria of the transmission symbols crosses a threshold and to adjust loop bandwidth in response to the criteria crossing the threshold.

2. The system of claim 1, wherein the criteria of the transmission symbols comprises a function of the amplitude signal or a function of the phase signal.

3. The system of claim 2, wherein the function of amplitude signal is selected from a group consisting of the amplitude signal, a first derivative of the amplitude signal, a second derivative of the amplitude signal, a square of the amplitude signal, and a derivative of the amplitude signal squared.

4. The system of claim 2, wherein the function of the phase signal is selected from the phase signal, and a derivative of the phase signal.

5. The system of claim 1, wherein the controller is operable to make a first adjustment to the loop bandwidth when the criteria of the transmission symbols crosses a first threshold and to make a second adjustment to the loop bandwidth when the criteria crosses a second threshold.

6. The system of claim 5, wherein the controller is operable to delay making the first adjustment by a programmable time delay.

7. The system of claim 1, wherein the controller is operable to make a first adjustment to the loop bandwidth when the criteria of the transmission symbols crosses a first threshold and to make a second adjustment to the loop bandwidth after a time delay interval.

8. The system of claim 7, wherein the controller is operable to delay making the first adjustment by a programmable time delay.
9. The system of claim 1, wherein the controller is operable to increase the loop bandwidth in response to detecting criteria of the transmission symbols being above the threshold.

10. The system of claim 1, wherein the controller is operable to decrease the loop bandwidth in response to detecting criteria of the transmission symbols being below the threshold.

11. The system of claim 1, wherein the PLL comprises:
   a frequency reference input for receiving a reference clock;
   a controllable oscillator for generating a radio frequency (RF) clock;
   a phase detection circuit operational to provide phase error samples indicative of phase difference between the RF clock and the reference clock for controlling the controllable oscillator; and
   a programmable filter connected to receive the phase error samples and connected to provide a filtered output to the controllable oscillator, the programmable filter comprising a proportional loop gain control having a programmable loop coefficient (alpha), wherein the loop bandwidth is adjustable in response to alpha.

12. The system of claim 11 wherein the programmable filter further comprises an integral loop gain control having a programmable loop coefficient (rho), wherein the loop bandwidth is adjustable in response to rho.

13. The system of claim 11, wherein the programmable filter further comprises one or more linear filters each having a programmable linear filter coefficient, coupled to first receive the phase error samples, wherein the loop bandwidth is adjustable in response to the linear filter coefficients.

14. The system of claim 13, wherein the programmable filter coefficients are configured such that at least one linear filter coefficient is changed before or after changing alpha.

15. The system of claim 11 wherein the programmable filter further comprises:
   an integral loop gain control having a programmable loop coefficient (rho), wherein the loop bandwidth is adjustable in response to rho;
   one or more linear filters each having a programmable linear filter coefficient, coupled to first receive the phase error samples, wherein the loop bandwidth is adjustable in response to the linear filter coefficients; and
   wherein the loop bandwidth is adjusted by changing one or more of a group consisting of the one or more programmable filter coefficients, alpha and rho.

16. The system of claim 15, wherein two or more of the group are changed simultaneously.

17. The system of claim 15, wherein one or more of the group are changed in multiple steps.

18. The system of claim 1 being a cellular telephone, wherein the PLL forms a local oscillator.

19. A method for operating digital system comprising a transmitter having a phase locked loop with a dynamically controllable bandwidth, comprising:
   performing vector modulation in response to transmission symbols, wherein each transmission symbol comprises an amplitude signal and a phase signal;
   detecting when a criteria of the transmission symbols crosses a threshold; and
   adjusting loop bandwidth in response to the criteria crossing the threshold.

20. The method of claim 19, wherein adjusting loop bandwidth comprises:
   making a first adjustment to the loop bandwidth when the criteria of the transmission symbols crosses a first threshold; and
   making a second adjustment to the loop bandwidth after a time delay interval.

21. The method of claim 19, wherein adjusting loop bandwidth comprises:
   making a first adjustment to the loop bandwidth when the criteria of the transmission symbols crosses a first threshold; and
   making a second adjustment to the loop bandwidth when the criteria crosses a second threshold.

22. The method of claim 19, wherein adjusting loop bandwidth comprises delaying making each adjustment by a programmable time delay.

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